LISARD: LabVIEW-Integrated Softcore Architecture for Reconfigurable Devices

Abstract - The development of industrial control and measurement systems is often based on modular commercial off-the-shelf hardware. Lately, for these platforms reconfigurable I/O modules with field-programmable gate-arrays (FPGA) have gained significance, since they allow the implementation of data processing functionality very close to the data acquisition interfaces. However, algorithm complexity and floating-point support are limited by FPGA resources and design methods. This contribution presents an application-specific configurably DSP software architecture built around a scalable double-precision floating-point arithmetic/logic unit. The core can be seamlessly utilized as a functional component in LabVIEW-based FPGA designs. A small study shows the performance of an example application implemented on the presented core in comparison to other embedded architectures.

Motivation: The Collaborative Research Centre 622 „Nano-positioning and Nano-measuring Machines“

A used development platform in the measurement and control domain is the PXI hardware and the graphical framework LabVIEW. In a typical application, the programmable hardware services are connected to the specific protocols of sensors/actuators and provide an adequate timing of data acquisition and actuation, while the controller CPU is used for computing, i.e., the communication latency from sensors to the controller CPU and back is actuation over the PXI backplane is approximately 30 µs. A relocation of floating-point algorithms to the FPGA is likely to reduce the transmission delays and thus decreasing the closed-loop period of control applications. Due to the limited support for floating-point hardware synthesis, efficient implementation of floating-point control algorithms into the FPGA using hardware description languages (HDL) is time consuming and expensive compared to CPU or DSP programming.

In the context of this research and development project high-performance data acquisition, processing and control algorithms have to be optimized implemented to satisfy challenging requirements for process precision under strict real-time conditions, i.e., the control system of a nanometer scale positioning and measuring machine incorporates multiple connected receiving fibers, with a target loop frequency of 100 kS/s, resulting in a processing time of 10 µs. To achieve the desired process quality double-precision floating-point computations are required.

The implementation of the Kalman filter consists of matrix operations on relatively small matrices with double-precision floating-point operations.

1. The execution performance contains the execution time per Kalman filter iteration and overall data-path latency including data transfer (Controller and LISARD implementations).
2. Runtime on the PCI controller has been determined for a native LabVIEW (generic and minimized) implementation. This filter results from task scheduling and compulsory data cache misses in the LabVIEW runtime environment. Comparison with the pure algorithms written in data-flow optimized C-code (DSL in LabVIEW) shows the significant overhead of the RT execution environment.

The LISARD component embedded in LabVIEW provides an adequate connection to the specific protocols of sensors/actuators and provides an adequate timing of data acquisition and actuation over the PXI backplane is approximately 30 µs. A relocation of floating-point algorithms to the FPGA is likely to reduce the transmission delays and thus decreasing the closed-loop period of control applications. Due to the limited support for floating-point hardware synthesis, efficient implementation of floating-point control algorithms into the FPGA using hardware description languages (HDL) is time consuming and expensive compared to CPU or DSP programming.

Conclusion - The software architecture for utilization as a function component in LabVIEW is highly configurable in terms of VLW-organisation, memory organization, operator selection and I/O-connectivity. The architecture is designed to process complex floating-point algorithms for real-time control applications on distributed FPGA platforms. The LISARD core is not supposed to substitute general purpose softcore CPUs, but to be used as a DSP core in a data flow design, or supplementing a CPU in an SoC.