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Hardware Implementation of a Mixed Analog-Digital Neural Network

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Abstract. This paper describes a hardware implementation of a firing neural network based on the models of Gerstner. It mainly consists of analog building blocks (neurons, synapses), but because of their digital interface and controlling it is a mixed-mode structure. The complete physical implementation of all components allows massive parallel and real time computation. The input data processing is located off-chip to enlarge the number of implementable neural networks.

1 Overview

The internal information processing of synapses and neurons is locally distributed. This simplifies the interconnection problem of the building blocks which is resolved by choosing a classical array architecture. This enables the realization of a wide variety of network topologies, ranging from fully connected toward multi-layer and locally connected architectures.
A neuron receives spatially and temporal added current pulses from its synapses placed in the column above. The neural activity A is a result of the comparison between the threshold and the capacitor voltages, charged by incoming current pulses. This binary activity is distributed to all synapses in a row. Aditionally, every neuron generates the pre- and postsynaptic history potentials H and H_d, respectively. Both are used in the synapses to implant a modified Hebbian learning algorithm to change the synaptic weights.
Each firing of the neuron is followed by a refractory period modeled by the refractionary circuit and lifting the firing threshold during a certain amount of time.
Every synapse consists of a learning circuitry (multiplier and charge pump), a weight storage capacitor with its refresh unit and a voltage-to-current converter. A single ended voltage-to-current converter generates the current output and the activity multiplier samples it thus generating the output pulses of the synapse.
The system has been currently simulated in its components at the algorithmic and electric domains using synthetic data. The synapse circuit has been initally implanted in a $2.4\mu m$ CMOS technology for verification and measurement. Implementations of a complete synapse and neuron in a $0.5\mu m$ CMOS are under way. Our aim is to develop a tool kit for design and implementation of free configurable neural networks including automatic place and route.
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