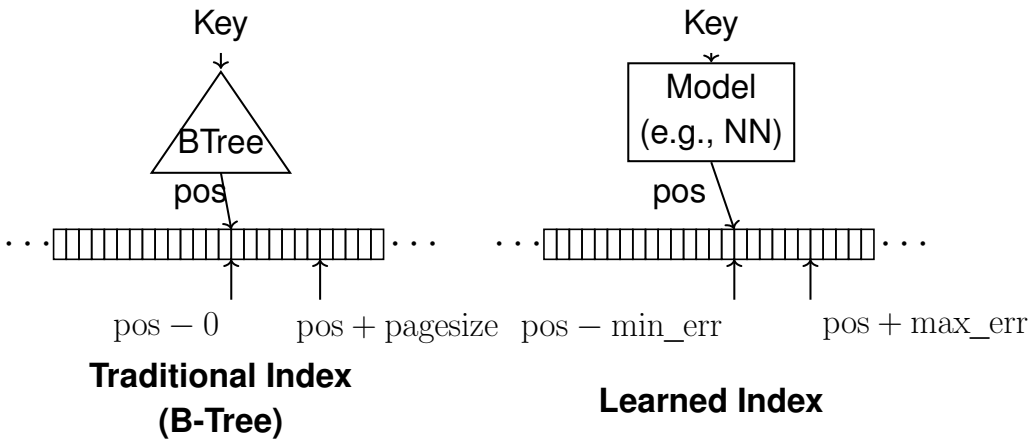
Accelerating Learned Index Using FPGAs (Hauptseminar)

Objective This research seminar focuses on hardware–software co-design and investigates how FPGAs can be leveraged to accelerate learned indexes.

Tasks

- Literature review.
- Analyze and compare different learned-index acceleration approaches.
- Investigate a suitable FPGA architecture.



Suggested Literature

- The Case for Learned Index Structures
- ALEX: An Updatable Adaptive Learned Index
- Learned Index Acceleration with FPGAs: A SMART Approach

Prerequisites:

Type of Work: Theory (70%), Conception (30%), Hauptseminar/Researchseminar

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