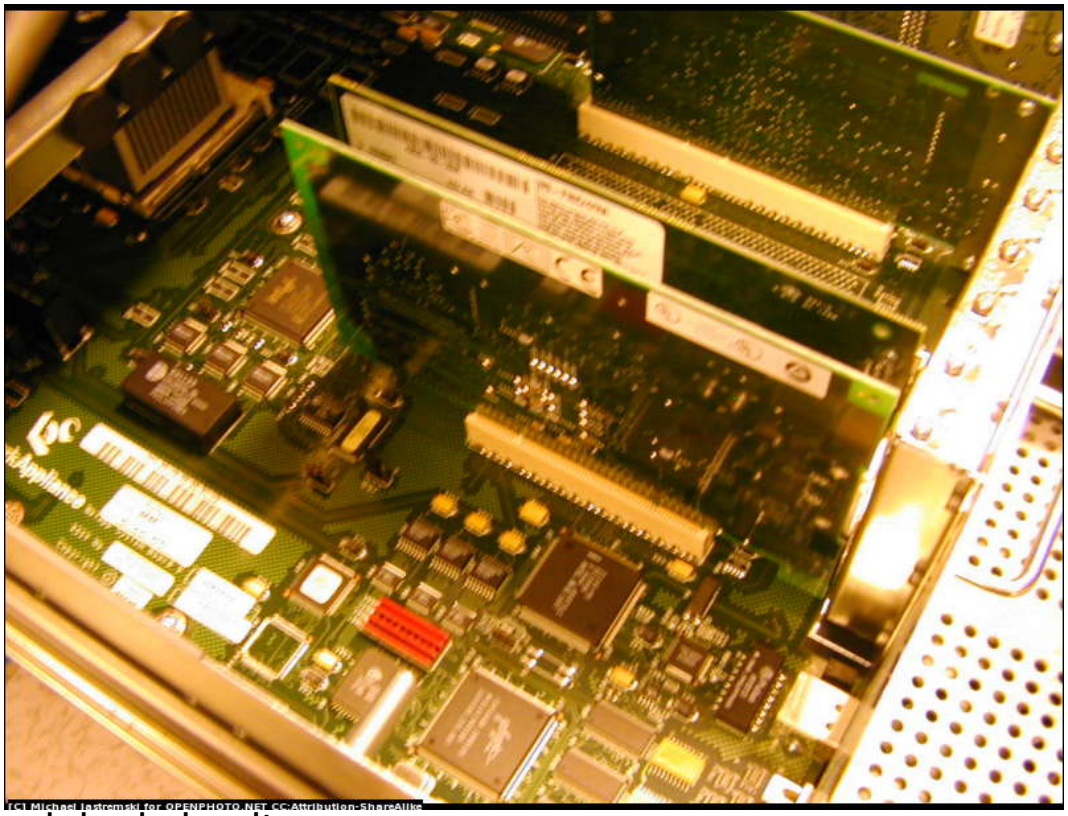
Efficient Design of Wave Pipelines on FPGAs

Pipelining is one of the most powerful methods to increase throughput in high-speed digital designs where the designer divides the combinational circuit in N stages, running concurrently, to achieve N times increase (theoretical) in throughput. In classical pipelines, Registers are included to guarantee a separation between the fastest and slowest moving data items. However, the same result can be obtained if all paths of the circuit have the same delay and wave pipeline effect is based on the same principal of equalization of all paths in order to allow several waves of data to travel along the circuit with a separation several times smaller than the maximum combinational delay. The avoidance of intermediate registers allows the WP to maintain the latency of the original circuit.



In this work, efficient design of wave pipelines on FPGAs will be explored and the benefits will be quantified using a case study.

Prerequisites: Good knowledge of Digital Logic Architecture and Design, Boolean Algebra

Type of Work: Master Thesis

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