

#### **Ilmenau Technical University**

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#### Software Performance Estimation for a Mission Level Design Flow

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- <sup>7</sup> Design Flow in MLDesigner
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- <sup>?</sup> Outlook



# Introduction

- <sup>?</sup> Electronic mixed hardware/software systems are raising in complexity at an exponential rate
- <sup>?</sup> Time-to-market should be descreased while the quality should stay the same or should become better
- <sup>?</sup> Therefore, several computer-aided design methodologies for detailed modeling of such systems (VHDL, C Code) were introduced in the last years

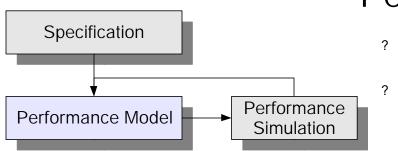


# Introduction

- <sup>?</sup> Nowadays the reached complexity makes detailed modeling impossible
- <sup>9</sup> Major problems rising with this complexity
  - <sup>?</sup> Immense modeling effort
  - <sup>7</sup> Simulation speed
- <sup>?</sup> Solution:
  - Raise level of abstraction without loosing too much of the accuracy



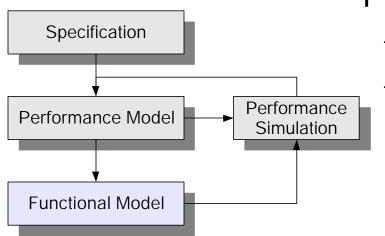
# Design Flow in MLDesigner



- <sup>?</sup> Performance Model:
  - <sup>7</sup> Describes the architecture
  - <sup>2</sup> Software is modeled as simple delays



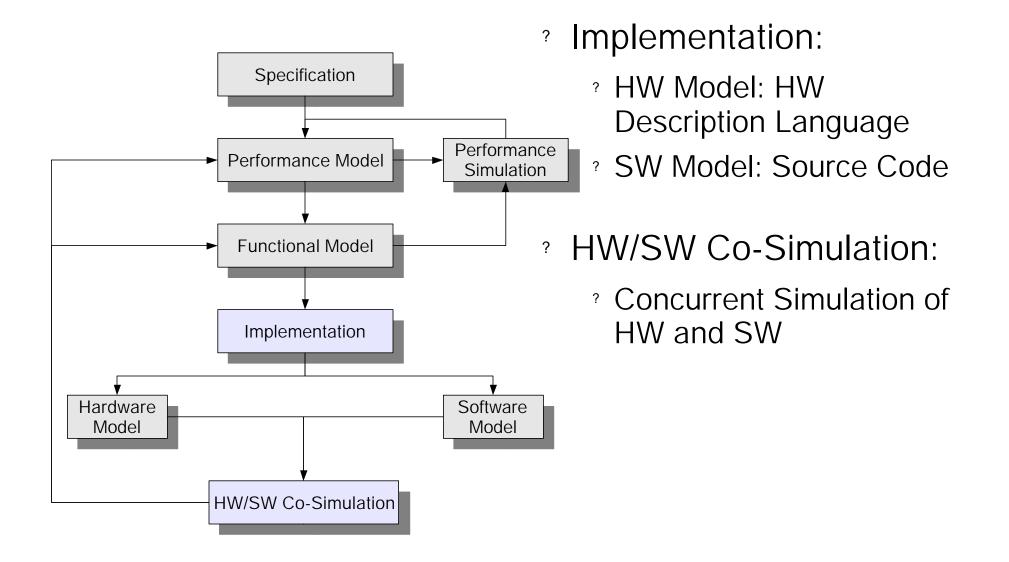
# Design Flow in MLDesigner



- <sup>?</sup> Functional Model:
  - <sup>?</sup> Describes the software
  - Independent of level of abstraction

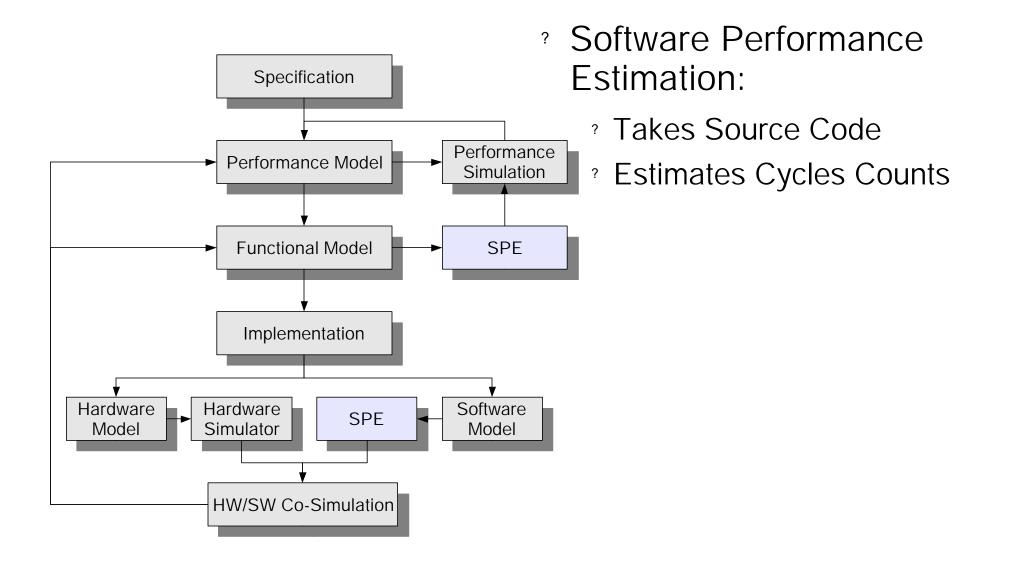


# Design Flow in MLDesigner





# MLDesigner Design Flow





### Software Performance Estimation

- <sup>?</sup> Definition
- <sup>?</sup> Approaches
- <sup>?</sup> General Work Flow
- <sup>?</sup> Work Flow in MLDesigner



# Definition

#### Software Performance Estimation

- <sup>9</sup> Is the estimation of the performance of a piece of software running on a specific target processor
- <sup>?</sup> Requirements: Source code must exist
- <sup>?</sup> Result: Cycle count





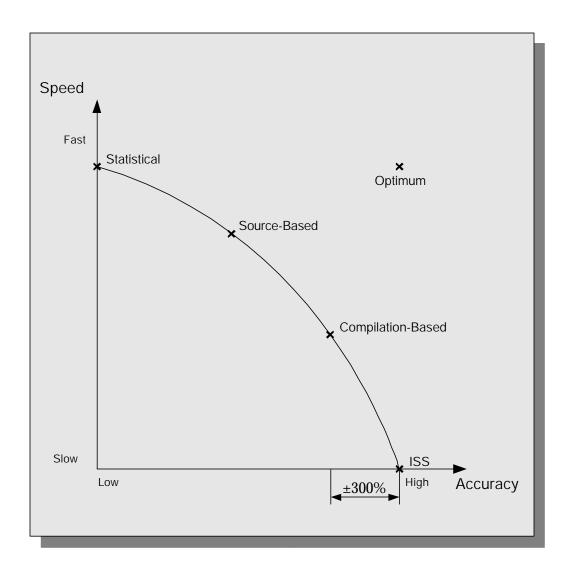
#### Approaches

- <sup>9</sup> Statistical Estimation
- <sup>?</sup> Source-Based Estimation
- <sup>7</sup> Compilation-Based Estimation
- <sup>7</sup> Estimation using Instruction Set Simulators



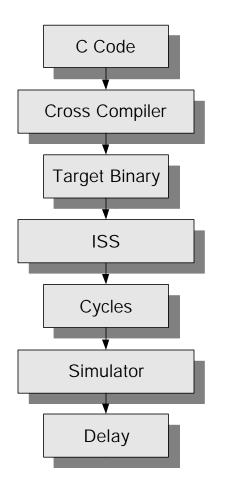


#### Approaches



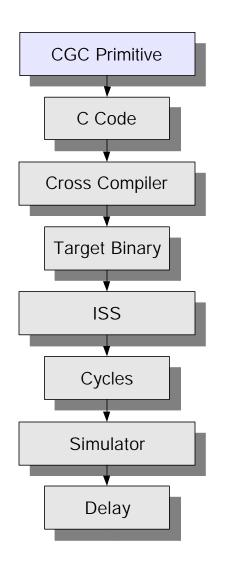


# General Work Flow



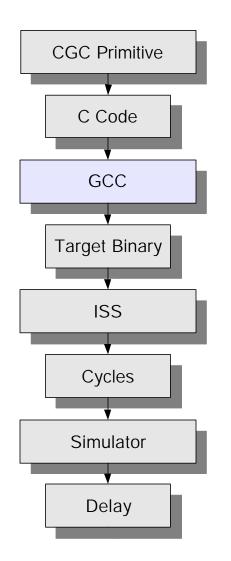
- Cross compiler generates target binary on host machine
- Instruction set simulator executes binary and calculates necessary cycles
- Simulator calculates delay caused by the code execution from cycles





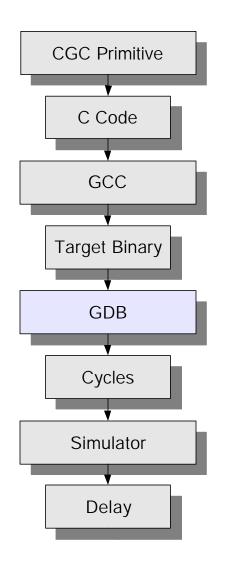
- CGC Domain is a code generation domain of MLDesigner for generation of C Source Code
- <sup>?</sup> CGC Co-Design target introduced





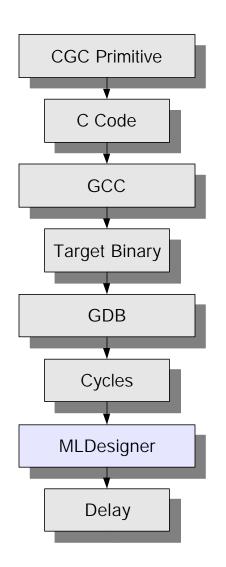
- <sup>7</sup> GNU Compiler Collection
- <sup>?</sup> C front-end of GCC is used for cross compiling
- <sup>9</sup> GCC containes cross-compilers for processors like ARM, Motorola 68k, PowerPC and MIPS





- <sup>?</sup> GNU Project Debugger
- <sup>9</sup> GDB is a collection of instruction set simulators
- <sup>9</sup> GDB containes fast instruction set simulators like the ARMulator for the ARM processor





Performes DE Simulation with delays calculated from cycles and processor speed





- <sup>?</sup> Problem Definition
- <sup>?</sup> Model Generation
- <sup>9</sup> Simulation and Results



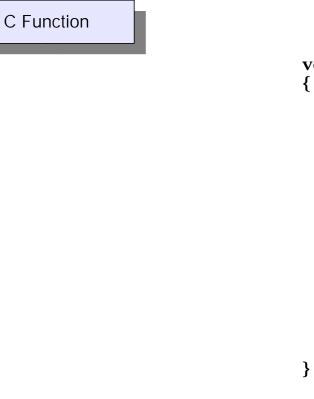
# **Problem Definition**

- Selection of an algorithm that has a runtime depending on the incoming data
   Fibonacci Algorithm
- ? 1. Task: How many Fibonacci numbers can be calculated by an ARM processor with 2.5 Mhz in one second
- <sup>9</sup> 2. Task: How do compiler optimizations influence the result





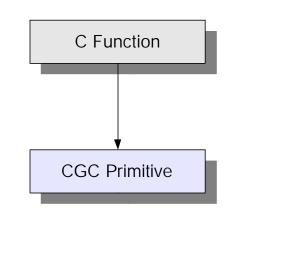
#### Model Generation



```
void fibonacci(int n)
{
    int data[n];
    int i, j, temp, c;
    i = 1;
    j = 0;
    for (c = 0; c < n; c++)
    {
        data[c] = i;
        temp = i + j;
        j = i;
        i = temp;
    }
}</pre>
```



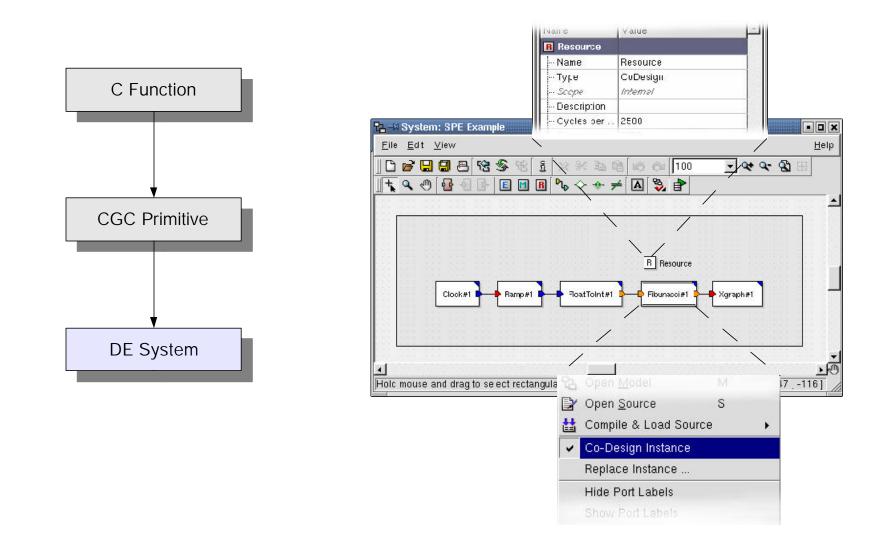
#### Model Generation



```
defprimitive
{
          {Fibonacci}
  name
  domain {CGC}
  . . .
  codeblock(fibonacci)
    int data[$ref(Input)];
    int i, j, temp, n;
    i = 1;
    i = 0;
    for (n = 0; n < \text{Sref(Input)}; n++)
       data[n] = i;
      temp = i + j;
      \mathbf{j} = \mathbf{i};
      i = temp;
    }
    $ref(0utput) = 1;
  }
  go
{
    addCode(fibonacci);
  }
}
```

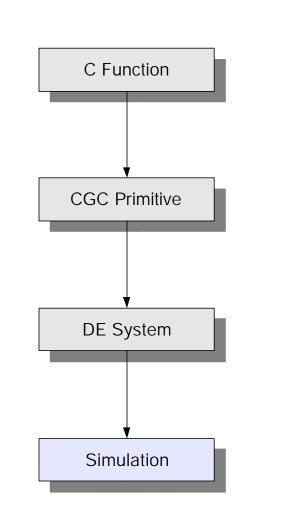


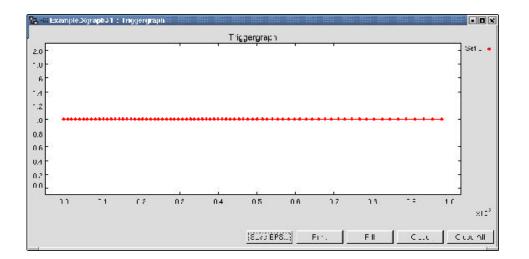
#### Model Generation





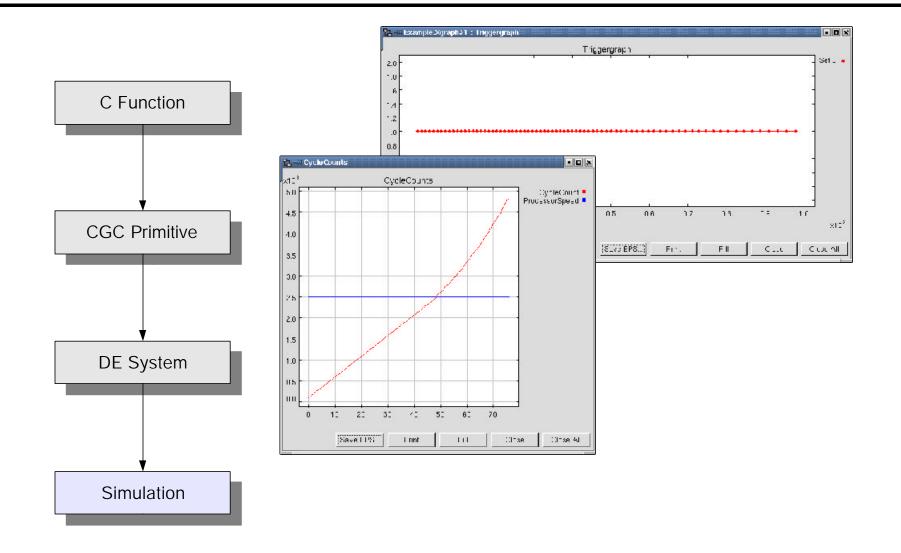
#### Simulation and Results





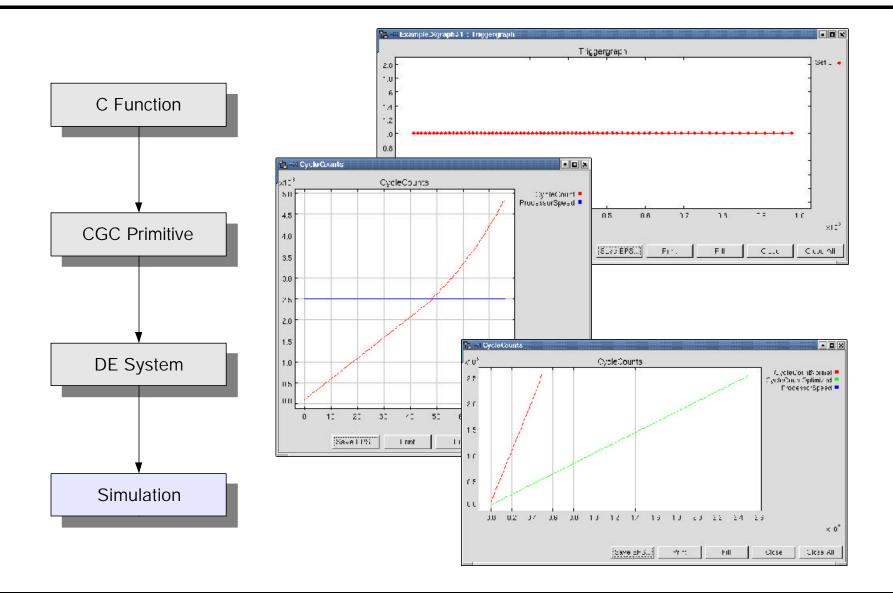


#### Simulation and Results





#### Simulation and Results







- <sup>a</sup> Abstract modeling of hardware and software including the according synthesis algorithms
  - <sup>?</sup> FSM
  - <sup>?</sup> UML
  - <sup>?</sup> SystemC
- Provide a structure of modeling capabilities at implementation level





#### Thank you for your attention!