Power Factor Compensation (PFC)

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The power factor (PF) is defined as the ratio between the active power and the apparent power of a system. If the current i and voltage v are periodic with period T, and $i, v \in \mathcal{L}_2[0,T)$, then the active power is defined by $\langle v, i \rangle = \frac{1}{T}\int_0^T v(t)i(t)dt$ (their inner product in $\mathcal{L}_2[0,T)$), and the apparent power is defined by $\|v\|\|i\|$. Hence,

$$\text{PF} = \frac{\langle v, i \rangle}{\|v\|\|i\|} .$$

When the voltage and the current are both purely sinusoidal, the PF is equal to the cosine of the phase angle θ between them. For sinusoidal voltage and non-sinusoidal current, we define I_1 as the fundamental component of the current, and I_{rms} as the RMS value of the current [1]. The PF depends of both the distortion factor of the waveform (defined as I_1/I_{rms}) and the displacement factor related to the phase angle ($cos\theta$, where θ is the phase difference between the fundamental component of the current and the voltage waveform), in the form

$$\text{PF} = \frac{I_1}{I_{rms}} cos\theta.$$

There are several reasons to seek a close to unity PF. First, the conduction losses in the grid depend on the current, which is proportional to the apparent power. Since only active power is used by the load, a PF < 1 will cause power losses due to the reactive power flowing through the grid. In addition, harmonics caused by the waveform distortion may disrupt other devices connected to the grid. The purpose of power factor compensation (PFC) is to minimize the input current distortion factor, and to minimize the phase difference between the voltage and current waves. This process is also called power factor correction or power factor conditioning (each abbreviated as PFC).

As in most power supplies the periods of the current and voltage waveforms are the same, and the peaks of the current coincide with the peaks of the voltage, the displacement factor is close to unity. Hence, the task of PFC is reduced to eliminating the higher order harmonics of the input current. The PF can thus be approximated by

$$\text{PF} \approx \frac{I_1}{I_{rms}} = \sqrt{\frac{1}{1 + \text{THD}^2}} ,$$

where THD is the "total harmonic distortion", which is the quadratic sum of amplitudes of the unwanted harmonics over the squared amplitude of the fundamental harmonic. Hence, an equivalent desirable quality of a PFC would be a THD close to zero.

Several standards have been established to limit the harmonic content of the input current of a power supply, the most common of them is EN61000-3-2 set by the European Union in 2001. Passive PFC circuits (built from transformers, diode and passive circuit elements) usually do not meet the standard criteria under a wide range of loads and for applications with higher power than approximately 400W [3]. In addition, passive PFC circuits require large and heavy magnetics. For this reason, an active PFC circuit is usually implemented in modern power supplies. Rectifier bridges and boost converters are most commonly used in active PFC, mostly due to their easy implementation and good performance.

There are several approaches to building a PFC based on boost converters, among them are critical conduction mode, continuous conduction mode, frequency clamped critical conduction mode and discontinuous conduction mode boost converters. Topologies of two boost stages are used in interleaved PFCs (common in low-profile form factor converters) where two stages operate out-of-phase in order to reduce the current ripple, and in bridgeless PFCs [5]. A myriad of other PFC topologies have been proposed in the literature, for various applications and with diverse properties.

An example – boost converter in a critical conduction mode

There are two control objectives for the boost converter in a PFC, namely: (1) attaining a nearly constant output voltage $V = V_{\text{ref}}$; (2) keeping the (short-time) average value of the input current i_g nearly proportional to the input voltage $u_g = A\sin(\omega t)$, thus obtaining a close to unity power factor.

There are several methods to build a PFC boost converter in continuous or discontinuous conduction modes. The boost converter depicted here operates in the critical conduction mode (CRM), also called border-line mode, as described in Gotfryd [2] and in Lai and Chen [4]. In the CRM operation, each current pulse of i_L has the form shown in Figure 2. During $0 \leq t < t_{on}$ in each pulse, the switch will be closed and the inductor current i_L will rise. During $t_{on} \leq t < T$ the switch will be open and the energy in the inductor will be released to the load and to the capacitor, causing i_L to fall to zero, since $V > u_r = |u_g|$.

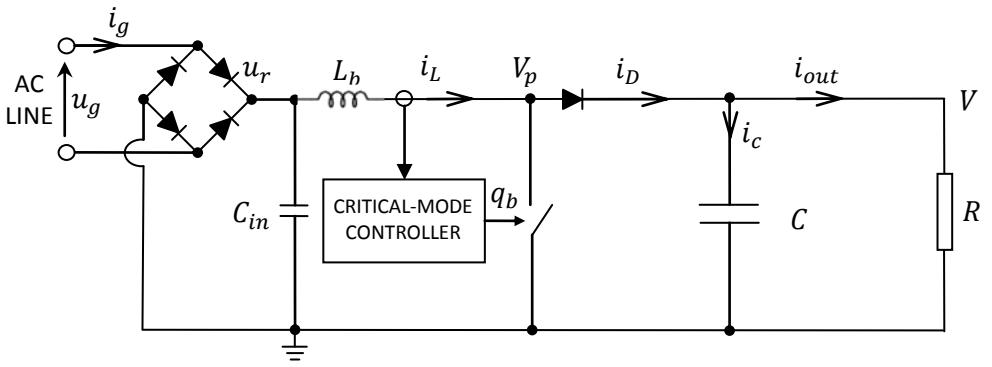

Fig. 1: A PFC using a boost converter.

When $i_L = 0$ is detected, the switch will close again, starting the next triangular pulse. Note that the switching frequency $1/T$ (which is variable) should be much greater than the grid frequency. The average current in a triangle is

$$\bar{i_L} = \frac{u_r}{2L_b} t_{on} \,. \tag{1}$$

Thus, to create an average current that is proportional to u_r, we hold t_{on} constant during each semi-cycle of the grid (from one zero crossing of the grid to the next). Then (according to (1)) the boost converter is seen from the grid like a resistor with resistance $\frac{2L_b}{t_{on}}$, which is a desirable behavior.

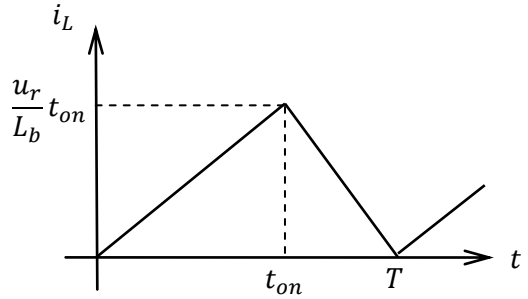

Fig. 2: The waveform of the inductor current, as required for critical conduction mode.

The diode is conducting only when the switch is open, hence its current i_D corresponds to the descending part of i_L in Figure 2 (for $t_{on} \le t < T$), and $i_D = 0$ otherwise. The average current of the diode is

$$\bar{i_D} = \frac{1}{T}(T - t_{on}) \frac{u_r}{2L_b} t_{on} \,. \tag{2}$$

From elementary considerations we have $-t_{on} = \frac{u_r}{V-u_r} t_{on}$, from where $T = \frac{V}{V-u_r} t_{on}$. Substituting this into (2) we obtain the (short-time) average current of the diode:

$$\bar{i_D} = \frac{u_r^2 t_{on}}{2L_b V}. \tag{3}$$

The expressions (1), (3) enable us to obtain an average model of the boost converter using a resistor and a current source that both depend on t_{on}, as shown in Figure 3.

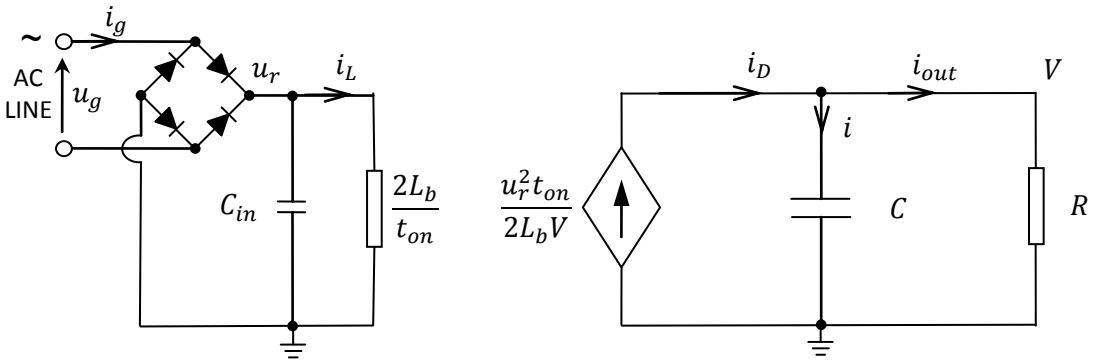

Fig. 3: The PFC from Figure 1 with the average model of the boost converter.

Finally, we discuss the power-up process of the converter. The circuit shown in Figure 3 must be connected to the grid at a proper time, where $|u_g| \in [u_{\min}, u_{\max}]$. The upper limit $u_{\max}$ is required in order to limit the in-rush current to the circuit at the time of connection. The maximal allowed in-rush current is determined by the properties of the switching components and the design specifications. When the circuit is connected below a certain lower limit $u_{\min}$, a somewhat more complicated power-up algorithm than presented below is required to deal with the slowly charging capacitor (which causes the problem of the descending inductor current, described below, to be more pronounced). In order to comply with these requirements, a mechanism that senses the phase of the grid and connects the circuit at a certain phase should be incorporated in the converter.

During power-up, there may be episodes where the slope of the descending inductor current (as shown in Figure 2) $\frac{u_r - V}{L_b}$ is too low, and the rising u_r may cause the inductor current not to reach zero before changing the sign of the slope. To prevent such episodes from damaging the power-up process, a protective logic should be incorporated in the control of the boost converter. A proposed logic is to close the switch of the boost converter when the inductor current starts rising (when supposed to be descending), in

addition to the case when i_L hits zero. This would cause a secondary in-rush current which will charge the capacitor and the boost converter will resume normal operation right afterwards as the descending slope of the inductor current will be steeper. This logic should allow this additional trigger only when the inductor current is below a certain limit ($\frac{u_r}{L_b} t_{on}$, either measured or calculated, can be used as a reference), otherwise accidental activations of the switch would cause the current to rise on undesired instances.

References

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