INTEGRATED WAFER-THROUGH FLUIDIC CONNECTIONS FOR SURFACE CHANNEL TECHNOLOGY

J. Groenesteijn¹, M.J. de Boer¹, T.S.J. Lammerink¹, J.C. Lötters¹,², R.J. Wiegerink¹

¹MESA+ Institute for Nanotechnology, University of Twente, The Netherlands
²Bronkhorst High-Tech BV, Ruurlo, The Netherlands

Abstract — A new method to integrate fluidic access to devices made by surface channel technology is proposed. The method uses a high aspect-ratio DRIE process for etching wafer through trenches to allows access to the front side of the surface channel device. LPCVD of TEOS is used as etch-stop and to define a reliable connection between channel and access trench during fabrication. The resulting connection is robust and increases design freedom for the surface channel technology. The complete fluid path has only one wetting material.

Keywords: surface channel technology, access holes

I – Introduction

Surface micro channel technology can be used for a wide variety of MEMS fluidic devices [1]. The ability to release these micro channels so they are freely suspended further increases their use. Possible applications are in the fields of fluid-mechanical resonance [2, 3] or gas chromatography [4]. The intended application is in the field of flow sensing [5, 6]. Typically, the channels in a micro Coriolis mass flow sensor have a diameter of 40 µm and a channel wall of less than 1.5 µm. For these sensors, it is important to have a reliable method to make strong connections between the channels and the macro world. The channels and access holes should be made from the same material for chemical inertness to the measured fluids. The access holes should be approximately the same size to prevent high fluidic resistance and dead volumes.

The access holes can be made in either the front or the back of the device. Front-side access holes allow only for small holes directly in the channel [1]. There are several disadvantages to front-side access holes. Any processing afterwards, like metalization and release of the channels, will suffer due to the holes at the topside of the wafer. It also increases the complexity of other top-side connections to the device after fabrication (eg. electrical connects or off-chip measurement devices) and vacuum sealing of the released devices. The main disadvantage is that, since the connection is directly on top of the channel, any forces or torques caused by assembly, handling or operation of the fluidic connection would be transferred directly to the buried channel membrane. This is therefore only suited to small fluid tubes with narrow top membranes.

The other option is to make the access holes through the wafer to the back-side of the device [7]. This means that the connection is to a strong, flat surface which provides a robust seating for an external connector. One advantage is that it leaves the front-side of the device open for other connections and will not interfere with top-side processing during the remaining part of the fabrication of the device (eg. metalization or release of the channels). However, it requires a wafer-through etch which limits the possibilities with respect to minimum dimensions of the access holes and channels and makes the fabrication more dependent of wafer-scale non-uniformities.

The intended application requires a channel radius which is too large to make a robust connection from the front-side, while they are too small to reliably make a connection from the back-side using the process in [7]. The new method presented here uses back-side access trenches and the fabrication process has been optimized to reduce the effect of non-uniformities, resulting in a fabrication process that can be used for a wide variety in dimensions for both the surface channels and access holes.

II – Front-side access holes

Front-side access holes are made by etching a hole

Figure 1: Schematic view of the fabrication process of the front-side access holes. The figure is not to scale. Left: cross-section along the channel. Right: cross-section perpendicular to the channel.

Figure 2: Schematic view of the design of front-side access holes. The relevant design parameters are shown.
schematically in figure 1. First, the channels are etched using an isotropic etch through small etch-slits. The channels are sealed by a silicon-rich-nitride (SiRN) layer which is deposited using low pressure chemical vapour deposition. The access holes have to be etched in the channels as the last step in the fabrication process of the device since the open holes will interfere with processing on the top-side of the wafer. The design to fabricate front-side access holes is schematically shown in figure 2. In the figure, \( w_{ah} \) is the width of the access hole and \( r_{sc} \) is the radius of the surface channel. Since the access hole is etched directly in the channel, \( w_{ah} \) should always be smaller than \( 2r_{sc} \) or the access hole will expose material outside the channel. When \( r_{sc} \) becomes too large, the membrane will become very fragile and can easily break during use or packaging, which means that this method can only be used with small surface channels.

III – Back-side access holes

Back-side access holes are made by etching a hole through the wafer. In [7], the process in figure 3 is used to connect surface channels to the outside world with round wafer-through access holes with a diameter of 50 µm. In this process, the access holes are etched first from the back-side. Then, a thick tetraethylorthosilicate (TEOS) oxide layer is deposited in the access hole to protect the hole during the channel etch. The channels are etched the same way as in figure 1 after which the TEOS is removed and a open connection between access hole and surface channel is created. The last step is to seal the etch-slits for the channels by a layer of SiRN.

![Figure 3: Overview of the fabrication process for round, back-side access holes. The overview is not to scale.](image)

Figure 4 shows a photo of access holes from the back-side successfully connected to surface channels on the top-side. At the top, five parallel channels are connected to each other by a channel perpendicular to them. The black dots in the middle of the channels are the 5x2 µm etch slits. The access holes are shown at the bottom of the figure. The photo gives a good impression of the small margins left for misalignment and variations in the wafer-through etch and the channel etch.

The access holes were designed to be adjacent the surface channels and are overlapping 2 µm. Figure 5(a, bottom) shows a schematic of the connection between the access holes and surface channels when the access hole is etched perfectly according to the profile in figure 5(a, top). \( r_{ah} \) is the radius of the access hole, \( r_{sc} \) is the radius of the surface channel and \( x \) is the heart-to-heart distance between the access hole and the channel. Three possible etch-results are shown.

![Figure 5: Schematic view of wafer-through access holes. Top: different etch profiles [8] and their connection to the surface channel. Bottom: top-view of the connection between the surface channel and the access holes resulting from the shown etch profiles. a) ideal result. b) etched too short. c) etched too long, with notching. The overview is not to scale.](image)

The figure shows that if \( x \) is larger than \( r_{ah} + r_{sc} \), the access holes will miss the channel and no connection is made. The lower limit of \( x \), that it should be larger than \( r_{ah} \), lies in the fabrication process of the channels. This lower limit is caused by the TEOS layer. The definition of the etch-slits in the SiRN with reactive ion etching will be different when there is TEOS underneath the SiRN instead of silicon, resulting in larger slits. These slits will then not be sealed during the last step and the channel will be leaky.

To etch the access holes through the wafer, a high aspect ratio Bosch etch is used. Ideally, an etch like that looks like the one in figure 5(a). However, in most cases when these holes are etched all over the wafer, some will not be etched far enough and look like the hole
in figure 5(b) and some will be over-etched as shown in figure 5(c), due to process inaccuracies and wafer-scale non-uniformities. The material used as etch-stop (SiRN) is non-conducting, meaning that notching will occur during over-etching [9].

These three different results lead to several problems in the design. The design is made for a certain \( r_{ah} \), but due to the variations shown in figure 5, there will be a spread in \( r_{ah} \) which changes the upper and lower limit of \( x \). When relatively large channels and access holes are used, the variation might not pose a problem. However, when the variation in access hole diameter comes into the range of the channel diameter, there will be no value for \( x \) for which it stays in the limits for both large and small access holes.

Figure 6 show the round access holes designed to have a diameter of 50 µm on different places of the same wafer which were etched using the process in figure 3. The photo is taken from the front-side of the wafer. The left photo shows holes with a diameter of 38 µm which corresponds to the etch profile shown in figure 5(b) when the bottom of the hole has just reached the SiRN. The right photo shows holes with a diameter of 63 µm which corresponds to the etch profile shown in figure 5(c). The circular patterns in the right photo show that the SiRN is etched.

![Figure 6: Access holes, viewed from the front-side of the wafer, at different places on the same wafer.](image)

**IV – Modified back-side access trenches**

A schematic overview of the new process can be seen in figure 7. Instead of using round holes, rectangular trenches are used. Using a rectangular trench instead of a round hole reduces the sensitivity to alignment errors and ensures a proper connection to the surface channel. The rounded bottom of the etched hole as shown in figure 5(b, top) remains, but will be flatter [8]. Figure 8 shows the design of the connection. \( r_{sc} \) is the radius of the surface channel, \( w_{ah} \) and \( l_{ah} \) are the width and length of the trench.

Steps a (channel fabrication) and b (access hole etch) have swapped places compared to figure 3. Making the channels before the access trenches ensures that the etch-slits for the channels will always be made in the SiRN layer while there is silicon underneath it.

During the wafer-through etching process, the channels are protected by a 1 µm thick layer of TEOS. This means that no extra silicon will be etched inside the channels during the wafer-through etch, resulting in a well-define connection between channel and access holes. The SiRN is not used as an etch stop anymore, which means that the ‘roofs’ of the access trenches are not etched during processing. The access trenches can be over-etched for the complete height of the surface channels before the SiRN top layer is damaged. The channels are approximately 35 µm high, meaning that, when a 525 µm thick wafer is used, a non-uniformity in the etch-rate of 7% can be compensated by over-etching, without causing problems. The silicon that is not etched away between the channels strengthens the ‘roof’ of the access hole. This order of etching gives the possibility to make an access hole that is fully overlapping with the surface channel and is thus free from the limits shown in figure 5.

**V – Results**

Figure 9(top) shows a photo from the front-side of a connection between surface channels and an access trench (shown as a dark area in the channels, outline by the dashed line). The SEM image in the middle shows a cross-section of such a connection at the horizontal red line, the SEM image at the bottom shows a cross-section along the vertical red line. The access trenches have a length of 300 µm and a width of 30 µm. The diameter...
of the surface channels is 35 µm. The images show that the trench connects to all five parallel channels with still some silicon left at the top. The trench crosses all channels, guaranteeing 100% connection, even with a slight misalignment.

![Image of successful connection between access trench and surface channel.](image)

**Figure 9:** Images of a successful connection between access trench and surface channel. Top: Photo taken from the front-side. The dashed line shows the outline of the access trench. Middle: Cross-section along the horizontal continuous line. Bottom: Cross-section along the vertical continuous line. The rough surface around the access hole and surface channels is a result of dicing the wafer. The effects at the top of the figure are due to charging of the TEOS sacrificial layer.

## VI – Conclusion

Fabrication methods for front- and back-side fluid access holes to surface channels have been discussed and a new method for back-side fluid access holes to surface channels is designed and tested. The new technology leaves the front side of the device open for other connections and does not disrupt any post-processing at the top-side of the wafer. A proper connection of the access trench to surface channels of a wide range of dimensions can be guaranteed. The effects of wafer-scale non-uniformities and mis-alignment has been reduced. The new technology provides a complete fluid path of only one material and improves the robustness of the connection between the surface channel and the access holes.

## References


