SILICON BASED SENSORS AND FUNCTIONAL COMPONENTS FABRICATED BY ICP-RIE CRYOGENIC DRY ETCHING

S. Merzsch¹, J. Kähler¹, H.S. Wasisto¹, L. Doering², U. Brand², E. Peiner¹ and A. Waag¹

¹Braunschweig University of Technology, Institute of Semiconductor Technology
Hans-Sommer-Str. 66, D-38106 Braunschweig, Germany
²Physikalisch-Technische Bundesanstalt (PTB), Nano- and Micrometrology
Bundesallee 100, D-38116 Braunschweig, Germany

Abstract — In this paper we present a broad summary on etching results achieved by inductively coupled plasma (ICP) cryogenic dry etching. Those structures include thin cantilevers, sensors for nano-force detection, vibration sensors and silicon grids. Due to high selectivity between resist and silicon ICP cryogenic dry etching offers the possibility to use thin photoresist masking. By varying the flux of oxygen and temperature, the etched shape was controlled in the individual cases. A challenge was the thermal coupling to keep the temperature at a low level even for high aspect ratios.

Keywords : Cryogenic reactive ion etching, Silicon on insulator, Silicon grid

I - Introduction

Micro electromechanical systems (MEMS) and nano electromechanical systems (NEMS) are available in a wide range today. The rapid progress in silicon micromachining within the last decades caused a wide spectrum of processing options. Surface and bulk micromachining can be achieved by using different etching methods. Wet etching of silicon is the oldest possibility and very common. In the field of research, it is still in use for creating NEMS structures [1]. Unfortunately for most applications, it includes a high grade of crystalline oriented anisotropy. Therefore, high aspect ratios in combination with vertical edges are only possible for <110> oriented substrates. Alternatively, realization of MEMS and NEMS can be done by dry etching using either the Bosch process or the cryogenic process. The former was invented by Lärmer and Schilp in 1994 [2]. It consists of a two-step alternating cycle including an etching step by applying SF₆ as the reactive gas and a surface passivation step based on C₄F₈. Drawbacks of this method are (1) a long dead time by switching gases leading to slow etch rates and (2) the contamination of the process chamber during the passivation using C₄F₈. As a result, periodical mechanical or chemical cleaning of the chamber is needed. An important attribute is the scalloping effect. During the first etching step, an etched pothole arises. One cycle later, another pothole has been etched below the first one, leaving a still passivated protrusion in between. In the progress all the way down to the etch bottom, there are ripples left behind. This is a huge drawback especially in the regime of NEMS.

Tachi et al. have firstly introduced a competitive method based on dry etching [3]. In contrast to the Bosch process, the cryogenic dry etching is a continuous process. SF₆ and O₂ are mixed inside the chamber to etch and passivate surfaces. The directed ions are cracking the passivation at the bottom due to their kinetic energy, while sidewalls are rarely affected. This process needs cooling to cryogenic temperatures to form a stable layer of SiOFₓ for sidewall passivation [4]. Complete desorption of the passivation layer takes place while warming up the sample to room temperature after the process was finished. No residues are left behind; neither in the chamber nor on the sample. The sidewall-quality does not suffer from scalloping, furthermore.

The challenges of the cryogenic process are explained related to recent examples of high-aspect-ratio structures for advanced sensor applications. As a novel approach in all cases the fabrication consists of multi-etching processes.

II - Experimental Details

Etching experiments have been done inside an SI 500C Dry Etcher (Fa. Sentech, Berlin). A planar triple antenna working at 13.56 MHz with a maximum power of 1200 W is placed in the upper part of the machine as the ICP source. The reaction chamber itself is separated from the source by two plates made of Al₂O₃ and quartz, respectively. A marginal distance of a few millimeters between those plates is provided. Whereas the top electrode is water-cooled, the bottom electrode can be defined to a chosen temperature by the interaction of a heating coil and a cooling system. As cooling agent nitrogen gas or even LN₂ are possible. The bottom electrode, made of stainless steel, is able to apply a maximum power of 300 W. The substrate carrier is clamped to the bottom electrode by a weighty mass ending up in a ring of Al₂O₃ pressing the carrier down. This ensures the contact between carrier lower side and the phosphorescent head of a glass fiber for temperature control. Around the fiber, Helium is fed into the chamber to assure a fast temperature response between electrode and carrier. Response from carrier to sample is assisted by a thermal paste. All in all this allows a stable heat transfer from the sample to the electrode. Nevertheless, the internal heat transfer of a sample will be addressed in this paper.

Silicon has been etched by an intermixture of SF₆ and O₂ in slightly varying portions as the processes needed. Different mask materials have been applied for the diverse units, including photoresist, metal and silicon dioxide.
III - Results and Discussion

A. Fabrication of cantilevers

Resonant cantilever sensors have large fields of applications. One example is the detection of airborne nanoparticles trapped on the cantilever by sensing the additional mass as a resonance shift. Those cantilevers have to meet several requirements. An extensive description of in-house developed self-sensing cantilevers and their utilizations can be read elsewhere [5, 6].

From the etching point of view, it is important to mention, that firstly a membrane is realized from the back side. This determines the thickness of the sensor. The cantilevers are freed by a second etching from the front side. In the given example, the temperature was kept at the relatively high level of -75 °C for both steps. While the front side is protected by resist, the side wall of the loose cantilever areas are affected by the plasma. Obviously the passivation layer has been vanished due to a poor thermal coupling. Figure 1 shows an entire cantilever and some detailed cut-outs as scanning electron microscope (SEM) images.

![Figure 1: A cantilever structure (upper part) and cut-outs from the free end, middle part and the clamp-end area. Whereas the passivation at the loose subzone degraded completely, the clamp-end area was still partly covered by the shielding layer due to a more intense heat transfer to the heat sink.](image1)

Besides the increased roughening an undercut has also been generated after breaking of the protection layer. A sharp border between intense roughness and almost smooth side walls are established in the range of the clamp-end area, where the thermal transport can be done faster (Fig. 1 lower right part). The middle part of the cantilever has been thinned down to 22 µm, whereas the free end has a thickness of 25 µm. This is caused by the deep etching profile while generating the membrane.

In principle, the silicon is etched homogeneously over a wide range. However, in this geometry the sidewalls are such narrow, that the edge effects for the plasma are also visibly acting in the central region of the membrane. For the manufacturing of parallel aligned front and back sides the membrane area has to be increased. Another approach is the utilization of silicon on insulator (SOI), where the buried oxide acts as a protective barrier against further etching.

B. Fabrication of micro-levers for nano-force detection

SOI has been used as material for production of a novel force sensor concerning micro- and nano-forces [7]. An area for force application is situated in between two meander-shaped regions with each consisting of seven lamellas. Around this configuration, a frame is including piezoresistive sensing elements. We are only focusing on the second etching step for producing the lamellas. Figure 2 presents a cut through a lamella just before finishing the etching process. Therefore, the etched surface is still observable.

![Figure 2: Cross section of a lamella along 270 µm showing areas of undercut, intact passivation for a lamella thickness of 40 µm along 175 µm and the actual etch bottom at a level of 255 µm.](image2)
The weaker passivation in the upper part of the lamella is clearly visible. As a result of diminution, above the most slender plane, the undercut is more intense than below. Except some spikes of beginning black silicon, the bottom surface has remained smooth. Another example is given by Figure 3. Part a) represents a complete formation. Typical force-deflection curves measured with a prototype sensor are given in part b) showing a nonlinearity of ± 0.3 % in the force range of 0 to 100 µN.

Figure 3: Mechanical part of a novel force sensor displayed by SEM (a) and measured force vs. deflection characteristic (b).

C. Advantages of DL-SOI for shaping a vibration sensor

For a more precise definition of structures, double layer SOI (DL-SOI) has been investigated for a high-temperature vibration sensor. As Figure 4 presents, it consists of a mass element (length = 700 µm, width = 400 µm, thickness = 50 µm) connected to a suspension comprising a full Wheatstone bridge as a piezoresistive strain gauge. A detailed description of the manufacturing of this sensor is explained by [8]. The buried silicon layer determines the cantilevers thickness of 6.2 µm. On top of a 0.2 µm oxide film a leakage-free Wheatstone bridge of four p-type resistors is realized by ICP-RIE etching of the top silicon layer. Resistor widths of 3 or 10 µm are shown in Figure 5. Rounding occurs due to limits of mask accuracy. Consequently, smaller structures are more affected. Back side etching consisted of two steps for preparing the mass and allowing a free deflection of the cantilever. Realized prototypes of this sensor were successfully tested according to the requirements of deep drilling projects such as geothermal power generation from deep geologic layers [8]. The fabricated Wheatstone bridge had excellent electrical properties such as a low noise of 0.7 mg/√Hz within a bandwidth of 1.6 kHz at 250 °C meeting the requirement of ≤ 1 mg/√Hz [9]. An example for the high signal stability of the sensor is given in Fig. 6. Here, the bridge voltage of the sensor is shown in dependence of the applied acceleration, i.e. 43 Hz corresponds to ± 30 g.

Figure 4: Front and back side of a vibration sensor in DL-SOI including mass, cantilever and a gold covered frame to assist the die-attach.

Figure 5: Two versions of bridge resistors with increased impact of similar process-conditioned rounding for 3 µm width.

Figure 6: Response of a vibration sensor to acceleration of different levels generated using a shaker.
D. Fabrication of particle filter grids.

A simple method to prevent a gas or fluid from large particles is to apply a filter. Grids for transmission electron microscopy are a commercially available solution for cavity diameters down to 0.6 µm. Unfortunately, those grids are very fragile, which makes their use for airborne particle filtering difficult. Therefore, ICP-RIE was applied to create grids from bulk silicon. The manufacturing process is shown in Figure 7.

**Figure 7:** Process sequence of silicon grid fabrication (upper) and SEM as well as photograph of a finished grid.

Silicon dioxide is thermally grown on a silicon wafer to be utilized as a grid mask by subsequent lithography and HF-Dip. A second lithography is done for preparing the rim at the front side. By ICP-etching the holes were transferred into the silicon. Before the back side was structured, the front has been protected by a resist layer to prevent mechanical deformation due to harsh contact to the carrier. This process flow has been chosen to prevent grid artifacts, i.e. mask undercut which had been expected due to the impaired release of the etching-induced heat through a membrane.

IV - Conclusion

In this paper ICP-RIE used for the fabrication of novel micromachined devices is described including mass, force and vibration sensors. Silicon structuring by ICP-RIE at cryogenic temperatures requires process-specific parameter variation. A critical value for side wall quality is the temperature. It has to be chosen at a level that guaranties an adequate cooling adapted to the design requirements.

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