High Aspect Ratio Dry Etching

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Several techniques exist to achieve anisotropy in plasma etching. One of the widely known methods is the reactive ion etching. For this technique, the flux of ions and chemically active radicals to the surface of the substrate must be adjusted in a way that the ion enhanced etching of the radicals is several times higher at the bottom of the trench than at the sidewalls. With this technique, vertical sidewalls up to several microns of depth and selectivities to oxide masks of up to 1:20 can be achieved. The low etch rate, however, is a problem for demanding applications, such as microelectronics, where depths of etching of up to 100 µm are required. By cooling down the substrate to -100 °C (typically), both anisotropy and selectivity of SF6/Oxygen based RIE processes can be increased. Applying this so-called "cryo etching" to inductively coupled plasmas even more increases the etching rate up to several microns per minute. At low temperatures, Oxygen and Fluor radicals deposit a non-volatile polymer film at the sidewalls and the bottom of the trench. The polymer film is removed only from the bottom of the trench, due to the impact of ions, which have a directed velocity distribution normal to the substrate surface, due to their acceleration in the sheath. Depending on the pressure and the DC bias voltage, however, there is also a certain fraction of ions with a velocity towards the sidewalls. The profile slope of the sidewalls hence is controlled by the ratio of polymer deposition rate versus polymer removal rate. If this ratio is 1, then as much polymer is removed as is deposited, hence the net change in polymer coverage of the sidewalls is zero, and the profiles are vertical. Therefore, by adjusting the flux of polymer forming radicals vs. flux of ions to the sidewalls, the profile can be controlled. By adjusting the gas flow rates and process parameters in order to obtain vertical sidewalls at the shadowed features, the profile slope of free-standing features will become negative (retrograde). It is therefore possible to obtain different depths of features on the same sample by using and applying this shadowing effect. If the shadowing features are narrow dots, these shadowing features will become underetched during the process, and will be released and removed from the substrate (see Fig. 1).

A way to obtain vertical profiles at room temperature is the gas chopping etch technique. The deposition of polymers and the etching of the sample are temporally separated. This is done by "chopping" from etching gases (SF6) to polymer forming gases (C4F8, CHF3, and the like). Due to the more degrees of freedom associated with gas chopping processes, such as cycle times or
different operating pressures during the etching and depositing cycles, a wider range of variation of the etching process is offered by gas chopping etching techniques. One method to adjust the profile slope for gas chopping processes is to ramp up the DC bias of the etching cycles during the process. In the start of the process, the DC bias is kept low, allowing for high selectivity even to "soft" resist masks. When, in certain depth, the profile would become positively sloped at these process parameter setting, the DC bias during the etching cycles is increased, thus the flux of ions to the bottom of the trenches increase, and the profile becomes vertical. Since the etching masks for many processes electrically insulating, the top of the sample becomes electrically charged during the etching process. The electrical charge on the mask, acts like an ion-optical lens which influences the trajectories of the ions. Depending on the pattern design and the process parameters, erosion of the sidewalls appears, due to increased ion flux to the sidewalls (see Fig. 2). If the bottom of the trenches also are insulating, as is the case for SOI wafers, the charging effect becomes increased, because in this case not only the charge of the mask, but also the charge of the buried oxide layer interact with the ions, increasing the effect. This is even more important if SOI wafers have to be substantially overetched when the feature sizes are very different (for instance, with micromechanical devices, as shown in Figures 3 and 4). However, these charging effects can be overcome by ramping up the DC bias in gas chopping processes.