Tool Supported Design of an Application-Specific Soft Microprocessor

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Topics

- Introduction
- Concept of the case study
- Overview of the soft microprocessor
- Design flow and tools
- Detail solutions
- Open questions
- Results and conclusion

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Introduction

Use of **FPGAs** (Field Programmable Gate Arrays) in Embedded Systems:

- Advantages in performance and flexibility
- Algorithms can be implemented directly or with soft microprocessors
- **Challenge:** Design processes
Concept of Case Study

- Embedding project: Special measuring machine
- Implementing closed-loop control algorithms
- Needs ~680 operations (DP floating point) per step
- Projected sampling rate: 300 kHz
- Case study investigates graphical design process using the LabVIEW tool
- Choice motivated by hardware support included
Overview of the soft microprocessor

- Problem specific processor architecture
- Configurable instruction set
- Omitting unneeded features
- Simple pipeline: No dependency logic
- Up to four cores, shared memory
Tool Supported Design of an Application-Specific Soft Microprocessor
Single-Core Setup

Program Memory -> Counter

Program Memory -> Instructions

Instructions -> Core

Core -> Data Mem. 1

Core -> Data Mem. 2

Data Mem. 1 -> In

Data Mem. 2 -> Out

In -> Addr. 1

Out -> Write Address

Out -> Read 2

Out -> Addr. 2
# Experimental Results

<table>
<thead>
<tr>
<th>6-Axes Control Algorithm</th>
<th>Instruction Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD, SUB</td>
<td>361</td>
</tr>
<tr>
<td>MUL</td>
<td>296</td>
</tr>
<tr>
<td>DIV</td>
<td>3</td>
</tr>
<tr>
<td>Type conversions</td>
<td>26</td>
</tr>
<tr>
<td>Transports</td>
<td>180</td>
</tr>
</tbody>
</table>

Double-precision floating point, clock frequency 120 MHz
## Experimental Results

<table>
<thead>
<tr>
<th>6-Axes Control Algorithm</th>
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<tbody>
<tr>
<td>Total</td>
<td>866</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Number of cores</th>
<th>1</th>
<th>2</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock cycle count</td>
<td>993</td>
<td>578</td>
<td>321</td>
</tr>
<tr>
<td>Execution time [µs]</td>
<td>8.28</td>
<td>4.82</td>
<td>2.68</td>
</tr>
</tbody>
</table>

Double-precision floating point, clock frequency 120 MHz
Design Flow and Tools

- All components use *LabView* design tool
- Except code design and operator library
- Fully integrated design process in preparation
Design Flow and Tools

Code Converter model:
- Source code parsing
- Machine code generation
- Pipeline and multi-core optimizations
Design Flow and Tools

Memory Init models:
- Memory images for program code and data
Processor Design model:
- Processor structure for FPGA implementation
- Configurable features
Configured Processor model:

- Configured processor design
- Translates into FPGA structure
Testbench model:

- Debugger functions
- Communication between FPGA and host
Detail solutions

- Give some impression about graphical approach
- Small model parts selected
- Total: ~50 LabVIEW worksheets
Detail Solutions

Code Converter detail
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Open questions

- Model based **software** design
- Extended **configurability**
- Model based **instruction set** synthesis
- **Compatibility** with embedding circuitry
Results and Conclusion

- **Design process** successfully investigated
- Advantages and weaknesses identified
- **Graphical approach** to classical compiler functions
- **Flexibility** of debugger environment
- **Goals** for further research outlined
Thank you for your kind attention