**Abstract**—Functional and formal verification are important methodologies for complex mixed-signal designs. But there exists a verification gap between the analog and digital blocks of a mixed-signal system. Our approach improves the verification process by creating mixed-signal assertions which are described by a combination of digital assertions and analog properties. The proposed method is a new assertion-based verification flow for designing mixed-signal circuits. The effectiveness of the approach is demonstrated on a Σ/Δ-converter.

### Digital Assertions
- Specification
- Model
- Implementation
- Property
- Assertions
- Design under Verification (DUV)
- Monitors

**Problem**
- Discrete time
- Signal triggered
- Boolean values
- Continuous time
- Time intervals
- Continuous values
- Ranges with inequalities

**Analog Properties**
- Continuous signal monitoring
- Continuous time consideration
- Frequency analysis

**Solution: combination of conditions**

### General definition of Mixed-Signal Assertions (MSA)

**Precondition**
- Analog → Digital

**Postcondition**
- Digital → Analog

### Characteristics (general)
- Including monitor points (digital/analog block)
- Specification language: PSL (property specification language)
- Using implication → operator for combining analog and digital conditions
- Interconnection verification

### Structure of MSA

**Analog Precondition**

\[ x(t) < 0.7 \text{ & } x(t) > -0.7 \]

**Digital Postcondition**

\[ \{ \text{next}_a[1:4] \} \]

**Temporal operator with interval**

**Digital signal**

### Case study

**Σ/Δ-Converter**

- \( f_{\text{an}} = 160\text{Hz} \)
- \( f_s = 20\text{Hz} \)
- \( k = 1.4 \)

**Mixed-Signal Assertions:**

1. \( x(t) < 0 \text{ & } x(t) > 1 \)
2. \( f(t) \in [0, 1] \)
3. \( \text{analog} \rightarrow \text{digital} \)

**Counterexample**

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