Partial Bitstreams generation tools/techniques: An overview

Partial Reconfiguration is an emerging technique for FPGA based applications to address issues like efficient area utilization of FPGAs in case of complex systems. For making a system partially reconfigurable, it is broken down into two parts: a static part and a dynamic partially reconfigurable part. The static design holds the parts of the system that need to be present and in operation all the time and they also usually provide the basic infrastructure to support the partial reconfiguration of the rest of the system. The dynamic part of the system consists of the system functions that occupy a specific dedicated area of the FPGA, referred to as the partial area, in a time multiplexed fashion.

As FPGAs are configured using bitstreams, the FPGA vendor tools, e.g. Xilinx, have a specific way of generating partial bitstreams that are ideal for island style reconfiguration on the FPGA. Those partial bitstreams contain the configuration bits for the partial area, as well as the information about the static part of the design to be implemented on the rest of the FGPA. Such partial bitstreams are not easily adaptable to the variety of partial reconfiguration techniques like slot and grid-style reconfiguration. In this assignment, the student will make a study of third-party tools for partial bitstream generation methods available in literature. A comparison should be made to assess which technique/tool can provide partial bitstreams that are well-suited for taking advantage of the features, like module relocation, that come with the slot and grid style partial reconfiguration. The techniques included in the study must also be compared with the different partial bitstream generation options by Xilinx.