IHS 3: Test of Digital Systems

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RT-Level Design

• data path and control path on RT-level
• RT level simulation
• Functional units (F1,..,F4)
• Register
• Multiplexer / Demultiplexer
Fault Modeling on High Level DDs

High-level DDs (RT-level):

- **M₁**
  - Function
  - 0: $M₁ = R₁$
  - 1: $M₁ = IN$

- **M₂**
  - Function
  - 0: $M₂ = R₁$
  - 1: $M₂ = IN$

- **M₃**
  - Function
  - 0: $M₃ = M₁ + R₂$
  - 1: $M₃ = IN$
  - 2: $M₃ = R₁$
  - 3: $M₃ = M₂ * R₂$

- **R₂**
  - Operator: Function
  - 0: Reset
  - 1: Hold
  - Load

- $y₁, y₂, y₃, y₄$ are the output variables for the DDs.

- The diagram illustrates the flow of signals through the DDs, with inputs and outputs labeled accordingly.
Fault Modeling on High Level DDs

**High-level DDs (RT-level):**

Terminal nodes represent:

RTL-statement faults:
- data storage, (e.g. #0)
- data transfer, (e.g. IN)
- data manipulation faults (e.g. $R_1*R_2$)

Nonterminal nodes represent:

RTL-statement faults:
- label,
- timing condition,
- logical condition,
- register decoding,
- operation decoding,
- control faults
High-Level DDs for a microprocessor (example):

### Instruction set:

- **I₁:** MVI A,D  \( A \leftarrow \text{IN} \)
- **I₂:** MOV R,A  \( R \leftarrow A \)
- **I₃:** MOV M,R  \( \text{OUT} \leftarrow R \)
- **I₄:** MOV M,A  \( \text{OUT} \leftarrow A \)
- **I₅:** MOV R,M  \( R \leftarrow \text{IN} \)
- **I₆:** MOV A,M  \( A \leftarrow \text{IN} \)
- **I₇:** ADD R  \( A \leftarrow A + R \)
- **I₈:** ORA R  \( A \leftarrow A \lor R \)
- **I₉:** ANA R  \( A \leftarrow A \land R \)
- **I₁₀:** CMA A  \( A \leftarrow \neg A \)

This slide from the Technical University Tallinn, ESTONIA, copyright 2000-2003 by Raimund Ubar, illustrates the concept of Decision Diagrams for Microprocessors with a high-level representation of a microprocessor's instruction set and a corresponding DD-model.
Hierarchical Test Generation

Transistor level

Logic level

RT Level

Component level

System level

Defect mapping

Hierarchical test (fault propagation)

Error
Experiments

• Use the example A+B/2 (average value)
• Find for each test method best parameters
  – Functional test
  – Deterministic test
  – Functional BIST
  – Logical BIST
  – Circular BIST
• Note them and compare results
High-Level Decision Diagrams Applet

- **Algorithm:** average
- **(A+B)/2**

- **a) high speed**
  - 2 operation units (F2, F3)
  - Add and Div in in 1 clock cycle
  - 4 steps
  - **Cost:** 83
High-Level Decision Diagrams Applet

- Algorithm: average
  - \((A+B)/2\)

- b) low cost
  - Only 1 Unit (F4)
  - 2 clock cycles for operation
  - 5 clocks
  - Cost: 73
High-Level Decision Diagrams Applet

- **Algorithm:** high speed average
- **(A+B)/2** (4 steps Cost: 83)

- **Simulation**
  - Load from Input Reg1
  - Load from Input Reg2
  - Add, Div and store in 1 clock cycle
  - Output and End

<table>
<thead>
<tr>
<th>Ad</th>
<th>Next</th>
<th>F1(in)</th>
<th>F2(in)</th>
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<th>F4</th>
<th>IN</th>
<th>F1</th>
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<th>F3</th>
<th>F4</th>
<th>F3(out)</th>
<th>F4</th>
<th>OUT</th>
<th>Input</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>C4</th>
<th>C5</th>
<th>C6</th>
<th>C7</th>
<th>C8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>REG1</td>
<td></td>
<td></td>
<td></td>
<td>A</td>
<td>X</td>
<td>X</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>REG2</td>
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<td></td>
<td></td>
<td>B</td>
<td>X</td>
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<td></td>
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</tr>
<tr>
<td>3</td>
<td>4</td>
<td>REG1</td>
<td>REG2</td>
<td></td>
<td></td>
<td>C</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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<td>X</td>
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<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>END</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REG3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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</tr>
</tbody>
</table>
Applets for Learning RT- Level Test

**Functional Test mode:**
The test vectors are operands results can be observed at the output, no extra test parts

**Deterministic Test mode:**
Gate level test for each FU separately, generate test vectors, local test panel, cumulative FC calculation

**BIST mode:**
Functional-, Logical- Circular Built In Self Test via extra test part: Test Pattern Generator and Signature analyzer
Functional Test

- The test vectors are operands, results can be observed at the output,
- no extra test parts needed
High-Level Decision Diagrams Applet

- Algorithm: average
- \((A+B)/2\)

- Funct.
- Test

![Diagram of high-level decision diagrams with a table showing test results.](image-url)
Deterministic Test

- Adder (F2)
  - Schematic level
  - Gate level test
  - Boolean derivation
  - SSBDDs
  - Path activation
  - Fault propagation
  - Fault observation
Deterministic Test

- Insert test vectors manually
- simulate the fault coverage of the vector (FC vec) and the sequence (FC)
Overview

1. Introduction
2. Theory: Boolean differential algebra
3. Theory: Decision diagrams
4. Fault modelling
5. Test generation
6. Fault simulation
7. Fault diagnosis
8. Testability measuring
9. Design for testability
10. Built in Self-Test
Built In Self Test (BIST)

- **Functional**
  - No additional part

- **Logical**
  - Additional TPG

- **Circular**
  - Additional TPG/SA
Built-In Self-Test

• Motivations for BIST:
  – Need for a cost-efficient testing
  – Doubts about the stuck-at fault model
  – Increasing difficulties with TPG (Test Pattern Generation)
  – Growing volume of test pattern data
  – Cost of ATE (Automatic Test Equipment)
  – Test application time
  – Gap between tester and UUT (Unit Under Test) speeds

• Drawbacks of BIST:
  – Additional pins and silicon area needed
  – Decreased reliability due to increased silicon area
  – Performance impact due to additional circuitry
  – Additional design time and cost
Built-In Self-Test in SoC

System-on-Chip testing

Test architecture components:
- Test pattern source & sink
- Test Access Mechanism
- Core test wrapper

Solutions:
- Off-chip solution
  - need for external ATE
- Combined solution
  - mostly on-chip, ATE needed for control
- On-chip solution
  - BIST
Built-In Self-Test Components

- BIST components:
  - Test pattern generator (TPG)
  - Test response analyzer (TRA)
- TPG & TRA are usually implemented as linear feedback shift registers (LFSR)
- Two widespread schemes:
  - test-per-scan
  - test-per-clock
Linear Feedback Shift Register (LFSR)

Pseudorandom Test generation by LFSR:

Polynomial: $P(x) = 1 + x^3 + x^4$
LFSR

- Find configurations of the LSFR
  - (Linear Feedback Shift Register) that generates optimal test vectors (TPG/SA)
- Parameters:
  - Feedback polynomial
  - Initial State
LFSR: Signature Analyser

Response string for Signature Analysis
Test Patterns (when generating tests)
Signature (when analyzing test responses)
Stimuli
BIST: Signature Analysis

**Aliasing:**

- Response

\[ k = 2^L \]

- Faulty response

- Correct response

\[ N \ll L \]

- All possible responses
- All possible signatures

\[ k = 2^N \]

- L - test length
- N - number of stages in Signature Analyzer

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BIST: Signature Analysis

- TPG / SA
  - Registers for LFSR
- Configure
  - Initial state
  - Polynom
- Parameters
  - TPG LFSR
  - SA LFSR
BIST: Signature Analysis

**Aliasing:**

- \( k = 2^L \) - number of different possible responses

No aliasing is possible for those strings with \( L - N \) leading zeros since they are represented by polynomials of degree \( N - 1 \) that are not divisible by characteristic polynomial of LFSR. There are \( 2^{L-N} \) such strings.

**Probability of aliasing:**

\[
P = \frac{2^{L-N} - 1}{2^L - 1} \quad \text{for} \quad L \gg 1 \quad \Rightarrow \quad P = \frac{1}{2^{-N}}
\]
BIST: Signature Analysis

Parallel Signature Analyzer:

Single Input Signature Analyser

Multiple Input Signature Analyser (MISR)
Built-In Self-Test

Signature calculating for multiple outputs:

- LFSR - Test Pattern Generator
- Combinational circuit
- Multiplexer
- LFSR - Signature analyzer

- LFSR - Test Pattern Generator
- Combinational circuit
- Multiplexer
- LFSR - Signature analyzer
Test-per-Clock BIST Architectures

BILBO - Built-In Logic Block Observer:
- LFSR - Test Pattern Generator
- Combinational circuit
- LFSR - Signature analyzer

CSTP - Circular Self-Test Path:
- LFSR - Test Pattern Generator & Signature analyser
- Combinational circuit
Reconfiguration for Self-Test

- Scan-IN
- Module
- Pseudorandom test generator
- Module
- Scan-OUT
- Test controller
- Signature Analyser
Test-per-Scan BIST Architectures

**STUMPS:**
Self-Testing Unit Using MISR and Parallel Shift Register Sequence Generator

**LOCST:** LSSD On-Chip Self-Test

![Diagram of STUMPS and LOCST architectures](image-url)
The main motivations of using random patterns are:
- low generation cost
- high initial efficiency

**Problem: low fault coverage**

If $\text{Reset} = 1$ signal has probability 0.5 then counter will not work and 1 for AND gate may never be produced.
Problems with BIST

The main motivations of using random patterns are:
- low generation cost
- high initial efficiency

**Problem:** low fault coverage

Possible patterns from LFSR:

Hard to test faults

Dream solution: find LFSR so that:
Store-and-Generate test architecture

The main motivations of using random patterns are:
- low generation cost
- high initial efficiency

**Problem:** low fault coverage

Long PR test:

Hard to test faults

Using many seeds:

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Store-and-Generate test architecture

- ROM contains test patterns for hard-to-test faults
- Each pattern $P_k$ in ROM serves as an initial state of the LFSR for test pattern generation (TPG)
- Counter 1 counts the number of pseudorandom patterns generated starting from $P_k$
- After finishing the cycle for Counter 2 is incremented for reading the next pattern $P_{k+1}$
Hybrid Built-In Self-Test

**Single test processes:**

- Hybrid test set contains a limited number of pseudorandom and deterministic vectors
- Pseudorandom test is improved by a stored test set which is specially generated to target the random resistant faults
- **Optimization**
Hybrid BIST for Multiple Cores

Embedded tester for testing multiple cores

[Diagram showing Embedded Tester connected to cores C2670, C3540, C1908, C880, and C1355 through BIST and Test access mechanism.]
Functional Self-Test

Register block → ALU → Signature analyser

N cycles → K*N → Fault simulator

K*N >> K

Functional test

Fault coverage

Test patterns are produced on-line during the working mode of the system.
Functional Hybrid Self-Test

- Register block
- ALU
- MUX
- M
- Automatic Test Pattern Generator
- Deterministic test set
- Random resistant faults
- Signature analyser
- Test patterns are stored in the memory
- Data
- K

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TURBO-TESTER: Low-Level TPG Tools

http://www.pld.ttu.ee/tt/

**Levels:**
- Gate
- Macro

**Methods:**
- Deterministic
- Random
- Genetic

**Fault models:**
- Stuck-at-faults
- Stuck-opens
- Delay faults

**Methods:**
- Single fault
- Parallel
- Deductive

**Design**
- Test Generation
- BIST Simulation

**Methods:**
- BILBO
- CSTP
- Store/Generate

**Test**
- Test Simulation
- Fault Table
- Test Optimization

**Fault Simulation**
- Fault Table
- Fault Diagnosis

**Fault Location**
Overview

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9. Design for testability
10. Built in Self-Test
Ad Hoc Design for Testability Techniques

Method of Test Points:

Block 1 is not observable, Block 2 is not controllable

Improving controllability and observability:

1- controllability:
CP = 0 - normal working mode
CP = 1 - controlling Block 2 with signal 1

0- controllability:
CP = 1 - normal working mode
CP = 0 - controlling Block 2 with signal 0
Ad Hoc Design for Testability Techniques

- Find
  - good additional observation points that improves the fault Coverage (FC)
- Find
  - optimal operands (= test vectors)
- Parameters:
  - Observation points
  - Operands
Ad Hoc Design for Testability Techniques

Method of Test Points:

Block 1 is not observable,
Block 2 is not controllable

Improving controllability:

Normal working mode:
CP1 = 0, CP2 = 1
Controlling Block 2 with 1:
CP1 = 1, CP2 = 1
Controlling Block 2 with 0:
CP2 = 0

Normal working mode:
CP2 = 0
Controlling Block 2 with 1:
CP1 = 1, CP2 = 1
Controlling Block 2 with 0:
CP1 = 0, CP2 = 1
Ad Hoc Design for Testability Techniques

Multiplexing monitor points:

To reduce the number of output pins for observing monitor points, multiplexer can be used:

$2^n$ observation points are replaced by a single output and $n$ inputs to address a selected observation point

_Disadvantage:_

only one observation point can be observed at a time
Ad Hoc Design for Testability Techniques

Demultiplexer for implementing control points:

To reduce the number of input pins for controlling testpoints, demultiplexer and a latch register can be used. 

N clock times are required between test vectors to set up the proper control values

N = 2^n
Time-sharing of outputs for monitoring

To reduce the number of output pins for observing monitor points, time-sharing of working outputs can be introduced: no additional outputs are needed.

To reduce the number of inputs, again counter or shift register can be used.

*Disadvantage:* only one observation point can be observed at a time.
To reduce the number of input pins for controlling test points, time-sharing of working inputs can be introduced.

To reduce the number of inputs for driving the address lines of demultiplexer, counter or shift register can be used.
Ad Hoc Design for Testability Techniques

Partitioning of large combinational circuits:

The time complexity of test generation and fault simulation grows faster than a linear function of circuit size. Partitioning of large circuits reduces these costs. I/O sharing of normal and testing modes is used. Three modes can be chosen:
- normal mode
- testing C1
- testing C2 (bolded lines)
Scan-Path design allows to control and observe internal flip-flops, which means that the task of sequential testing has been transformed to the task of testing a combinational circuit.

- **T = 0** - normal working mode
- **T = 1** - scan mode

**Normal mode**: flip-flops are connected to the combinational circuit.

**Test mode**: flip-flops are disconnected from the combinational circuit and connected to each other to form a shift register.
Two possibilities for improving controllability/observability
Parallel Scan-Path

In parallel scan path flip-flops can be organized in more than one scan chain
Hierarchical test generation with Scan-Path:

Control Part

Data Part

Bus
Logical BIST

- Test Microprogram
- Parameters
  - Program steps
  - Used registers
  - Tested functions
Random Access Scan

In random access scan each flip-flop in a logic network is selected individually by an address for control and observation of its state.
Boundary Scan Standard
Conclusions

- **Self-Test** of modules (components) is important, but is not the *Panacea*
- **Hierarchical and Functional Test** have the same importance
- **Functional Fault Model** is a universal means for mapping defects, faults and errors from level to level, providing a formal basis for hierarchical approach
- **Decision Diagrams** can be used successfully not only at logical levels, but also at higher RTL or behavioral levels
References

• **Contact data:**
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Testability of Design Types

General important relationships:

- T (Sequential logic) < T (Combinational logic)
  Solutions: Scan-Path design strategy

- T (Control logic) < T (Data path)
  Solutions: Data-Flow design, Scan-Path design strategies

- T (Random logic) < T (Structured logic)
  Solutions: Bus-oriented design, Core-oriented design

- T (Asynchronous design) < T (Synchronous design)

- T: Testability
Testability Estimations for Circuit Types

Circuits less controllable

- Decoders
- Circuits with feedback
- Counters
- Clock generators
- Oscillators
- Self-timing circuits
- Self-resetting circuits

Circuits less observable

- Circuits with feedback
- Embedded
  - RAMs
  - ROMs
  - PLAs
- Error-checking circuits
- Circuits with redundant nodes
Testability Measures

Evaluation of testability:

- Controllability
  - $C_0 (i)$
  - $C_1 (j)$
- Observability
  - $O_Y (k)$
  - $O_Z (k)$
- Testability

Controllability for 1 needed

Defect
Probability of detecting $1/p^{60}$
Probabilistic Testability Measures

Controllability calculation:
Value: minimum number of nodes that must be set in order to produce 0 or 1

For inputs: \( C_0(i) = p(x_i=0) \) \( C_1(i) = p(x_i=1) = 1 - p(x_i=0) \)

For other signals: recursive calculation rules:

\[
p_y = 1 - p_x
\]

\[
p_y = p_{x_1} p_{x_2}
\]

\[
p_y = 1 - (1 - p_{x_1})(1 - p_{x_2})
\]

\[
p_y = \prod_{i=1}^{n} p_{x_i}
\]

\[
p_y = 1 - \prod_{i=1}^{n} (1 - p_{x_i})
\]
Probabilistic Testability Measures

Probabilities of reconverging fanouts:

\[ p_y = (1 - p_{x1})p_{x2} + (1 - p_{x2})p_{x1} \]
\[ = 0.25 + 0.25 = 0.5 \]

\[ p_y = 1 - (1 - p_a)(1 - p_b) \]
\[ = 1 - 0.75 \times 0.75 = 0.44 \]

Signal correlations:

\[ p_y = p_x \cdot p_x = p_x^2 \]
Calculation of Signal Probabilities

**Parker - McCluskey algorithm:**

\[ p_y = 1 - (1 - p_a)(1 - p_b) = \]
\[ = 1 - (1 - p_{x1}(1 - p_{x2}))(1 - p_{x2}(1 - p_{x1})) = \]
\[ = 1 - (1 - p_{x1} + p_{x1}p_{x2})(1 - p_{x2} + p_{x1}p_{x2}) = \]
\[ = 1 - (1 - p_{x2} + p_{x1}p_{x2} - p_{x1} + p_{x1}p_{x2} + p_{x1}p_{x2}^2 + p_{x1}^2p_{x2} + p_{x1}p_{x2}^2 + p_{x1}^2p_{x2}^2) = \]
\[ = 1 - (1 - p_{x2} + p_{x1}p_{x2} - p_{x1} + p_{x1}p_{x2} + p_{x1}p_{x2} - p_{x1}p_{x2} + p_{x1}p_{x2}^2 + p_{x1}^2p_{x2} + p_{x1}p_{x2}^2 + p_{x1}^2p_{x2}^2) = \]
\[ = p_{x2} - p_{x1}p_{x2} + p_{x1} - p_{x1}p_{x2} + p_{x1}p_{x2} - p_{x1}p_{x2} + p_{x1}p_{x2} - p_{x1}p_{x2} = \]
\[ = p_{x1} + p_{x2} - 2p_{x1}p_{x2} = 0.5 \]
Calculation of Signal Probabilities

**Straightforward methods:**

\[
\begin{align*}
\text{Calculation gate by gate:} \\
p_a &= 1 - p_1p_2 = 0.75, \\
p_b &= 0.75, p_c = 0.4375, p_y = 0.22 \\
\text{Parker - McCluskey algorithm:} \\
p_y &= p_c p_2 = (1 - p_a p_b) p_2 = \\
&= (1 - (1 - p_1 p_2) (1 - p_2 p_3)) p_2 = \\
&= p_1 p_2^2 + p_2^2 p_3 - p_1 p_2^3 p_3 = \\
&= p_1 p_2 + p_2 p_3 - p_1 p_2 p_3 = 0.38
\end{align*}
\]

For all inputs: \(p_k = 1/2\)