Surface patterning using templates: concept, properties and device applications

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Received 7th April 2010
DOI: 10.1039/b924854b

Surface nano-patterns on substrates are the fundamental structures of various nano-devices. Template-based surface nano-patterning techniques are highly efficient methods in realizing different surface nano-patterns. The time-saving and low-cost fabrication processes of the template-based surface patterning are highly desirable for industry in fabricating different kinds of nano-devices. This tutorial review summarizes the recent advancements in the field of template-based surface nano-patterning, especially focusing on three templates prepared using self-assembly processes: ultra-thin alumina membranes, monolayer polystyrene sphere arrays, and block copolymer patterns. The basic concepts, the general fabrication processes, the structure-related properties, and the device applications of these template-based surface nano-patterning techniques are introduced.

1. Introduction
Multifunctional surface patterns on substrates are the foundation of semiconductor devices. To improve the performance of an integrated device, size-minimization of surface patterns (device miniaturization) is technologically required by industry to reduce the size of the individual device component. Thus, the present smallest feature size of integrated circuits has decreased to several tens of nanometres. This is the reason why surface nano-patterning became one of the most intensively studied topics in the past decade in the fields of material science and engineering. In order to control the properties of surface nanostructures and hence devices, it is mandatory to fabricate surface nano-patterns with adjustable structural parameters. Moreover, time-saving and low-cost fabrication processes of surface nanostructures are highly desirable for device applications.

There are different nano-structuring techniques in patterning various building blocks (e.g., nanodots, nanopillars, nanotubes, ...
nano-spheres) on the surface of substrates, mainly including lithographic methods, nano-imprinting and replica molding processes, scanning probe microscope (SPM) writing techniques, and template-based methods. Among these techniques, surface patterning methods using templates prepared by self-assembly processes are highly efficient in preparing surface nanostructures. The template-based methods are time-saving approaches with low equipment cost in fabricating large-scale ordered arrays of surface structures compared to lithographic methods (especially electron-beam lithography) and SPM writing processes.

So far many kinds of templates have been used to prepare surface patterns on substrates (usually semiconductor wafers). The motivation of using templates in creating surface patterns is to transfer the structural features of the templates to the surface structures on substrates, obtaining surface patterns with similar morphological features to those of the templates. Templates can be used for different purposes in the patterning processes, including masks for etching, evaporation, and reaction, substrates for growth and supporting, and molds for replication. There are three widely-used templates that are prepared using self-assembly processes: ultra-thin alumina membranes (UTAMs), monolayer polystyrene (PS) sphere arrays, and block copolymer (BCP) patterns. The surface patterns synthesized using these templates have promising device application potentials due to the low-cost and time-saving fabrication processes of surface structures. As three major patterning templates derived from self-assembly processes, PS, BCP, and UTAM templates have their own unique aspects. First, the feature size of the building blocks of the surface patterns prepared using BCP, UTAM, and PS templates can be adjusted within the range of about 5–50 nm, 5–500 nm, and 50 nm–4.5 µm, respectively. This means that these three template-based surface patterning techniques can cover the whole range from the quantum size to the nanometre size and finally to the micrometre size range. Second, PS sphere arrays and BCP patterns are soft (polymer) templates that can be removed by either chemical dissolution or burning processes, while UTAM is a hard template of metallic oxide that can only be removed by chemical dissolution. Moreover, these templates have different morphological features: the UTAM porous template has parallel-aligned cylindrical nano-pores, the PS template is a monolayer of closely-packed arrays of spheres, and the BCP template has some special shapes such as lamella. Diverse surface structures have been prepared based on the different structural and morphological features of these templates.

Due to the above-mentioned features of template-prepared surface nanostructures, surface patterning using templates is a very important research direction within the fields of surface nano-structuring and nano-devices. There are some review articles introducing surface patterning using templates. However, reviews that generally summarize the template-based surface patterning processes are still lacking. Moreover, many recent important achievements within the past few years also require a review to summarize the new improvements of template-based surface patterning techniques.

In this review, we give a systematic overview on the surface nano-patterning techniques using the above-mentioned three templates. Besides the basic concepts and the general fabrication processes of the template-based surface patterning, we will focus on the recent advancements of the structure-related properties and the device applications of the template-prepared surface patterns. First, recent processes regarding surface patterning processes using UTAM (Section 2), PS (Section 3), and BCP (Section 4) templates are introduced. Subsequently, device application aspects of surface nano-structures prepared using templates are discussed in Section 5. Finally, Section 6 gives a brief summary of the template surface nano-patterning together with a short outlook on future developments.

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2. UTAM surface nano-patterning

2.1 Concept of nano-patterning processes using UTAMs

UTAM surface nano-patterning is an emerging surface nanostructuring technique, in which UTAMs are used as deposition,5–19 etching,20–25 or replication masks.26–29 As a special type of anodic alumina membranes, UTAM is a through-hole membrane with small thickness of about several hundred nanometres. UTAMs can be placed or fabricated on substrates so as to synthesize ordered arrays of surface nanostructures.

Fig. 1 summarizes the fabrication routes of the UTAM surface nano-patterning. Two different types of UTAMs can be prepared on substrates. Using a two-step anodization process on a high-purity aluminium (Al) foil, an UTAM can be prepared using a very short second-anodization time. After removing the Al foil and a barrier layer at the backside of the sample, the UTAM is transferred to the surface of a substrate, forming an attached UTAM (A1 → A2 → A3). UTAMs can also be prepared directly on substrates. A high-purity Al layer is first evaporated on a substrate. Then a connected UTAM is prepared on the substrate by anodization processes (B). After obtaining UTAMs on substrates, regular arrays of different surface nanostructures can be prepared by six fabrication routes (Routes I–VI). Using vacuum evaporation processes (e.g., thermal and E-beam evaporation, sputtering process) followed by the removal of the UTAM, nanodot arrays are fabricated on substrates (Route I: a1 → a2). In the meantime, the evaporated material also deposits on the top of the UTAM, forming a porous top layer. Further evaporation will close the pores of this top layer (i.e., capping the UTAM pores completely), resulting in nanoring structures on the bottom surface of the top layer (a3). Finally this nanoring-featured top layer can be transferred to the surface of another substrate (Route II: a1 → a3 → a4). Using evaporation, wet-chemical or polymerization process, nanopillar arrays can be synthesized on the top of an UTAM (b1). The nanopillar arrays can also be attached on another substrate at the backside and be separated from the UTAM (Route III: b1 → b2 → b3). Another fabrication route is to use reactive ion or plasma etching processes to excavate nanoholes on substrates (c1).

![Fig. 1 Schematic illustration (cross-sectional view) of the UTAM surface nano-patterning. Two types of UTAMs are prepared on substrates: attached UTAM (A1 → A2 → A3) and connected UTAM (B). Different surface nanostructures are prepared using six fabrication routes (Routes I–VI): (I) nanodot arrays (a1 → a2), a1: evaporation, a2: removing UTAM; (II) nanoring arrays (a1 → a3 → a4), a3: further evaporation until the UTAM pores are fully capped, a4: removal of the top layer and transfer to another substrate; (III) nanopillar arrays (b1 → b2 → b3), b1: fill in the UTAM pores, b2: adhere another substrate on the top, b3: removing UTAM; (IV) nanohole arrays (c1 → c2), c1: ion or plasma etching, c2: removing UTAM; (V) nanopillar arrays (d1 → d2 → d3), d1: anodization of Al to prepare a connected UTAM on a metal-covered substrate, d2: electrochemical deposition or anodization to prepare nanopillars, d3: removing UTAM; (VI) quantum-sized nanodot arrays (e1 → e2 → e3), e1: quantum-sized pore-opening on the barrier layer of UTAM by a controllable etching process, e2: attach the UTAM on a substrate followed with evaporation process, e3: removing UTAM.](https://example.com/fig1.png)
After removing the UTAM, ordered arrays of nanoholes on substrates are obtained (Route IV: c1 → c2). Nanopillar arrays of semiconductors, metals, and oxides can also be synthesized (Route V: d1 → d2 → d3) using a connected UTAM on a substrate covered by a thin metal layer (d1). After forming a connected UTAM, nanopillars can be prepared by an electrochemical process or further anodization on the metal interlayer (d2–d3). Recently, a new fabrication route (Route VI: e1 → e2 → e3) was proposed and it can be used to synthesize quantum dot arrays on substrates using UTAMs with quantum-sized pore-openings on the barrier layer.

Based on the above, regularly arrays of different surface nanostructures including nano- and quantum-dots, nanorings, nanoholes, and nanopillars can be fabricated using the UTAM surface patterning technique. The pore diameter and spacing of UTAMs can be adjusted within the range of about 5–300 nm and 15–500 nm, respectively. Thus the size and spacing of the UTAM-prepared surface patterns can be tuned in similar size ranges. After the formation of surface nanostructures, UTAMs can be selectively removed by acidic or alkali solutions, depending on the materials of surface structures.

From the pioneering work of Masuda and Satoh in 1996,1 different types of materials have been fabricated into surface nano-patterns using the UTAM nano-patterning technique, including semiconductors, metals, and oxides.5–10 Besides the controllable size and spacing of the UTAM-prepared surface structures, their shape can be adjusted by changing the pore aspect ratio of UTAMs.9 Such controllability of the structural parameters allows tuning the properties of surface nano-patterns.10 Moreover, some advanced composite structures can be prepared using the UTAM technique, such as metal/oxide core-shell nanodots oxidized from metal nanodot arrays,10 high-quality device-level GaN layers grown on ordered GaN nano-hole arrays,20 and nano-capacitors based on nano-hole arrays.21 The advantageous features of the UTAM nano-patterning technique, such as the tunable structural parameters and large pattern area (>1 cm²), high throughput and low equipment costs of the fabrication processes, general applicability in fabricating different nanostructures, make the technique suitable to fabricate ordered surface nanostructures with tuneable properties and hence nano-devices with good performance.

2.2 Nanodot arrays

Nanodots (including quantum dots) are one of the most important building blocks of surface patterns for diverse device applications. The UTAM surface nano-patterning has been recognized as a very efficient way in fabricating arrayed nanodots with well-defined structures that are highly favorable for different property investigations, such as surface enhanced Raman scattering (SERS) properties. Masuda et al. fabricated Au nanodot arrays using the fabrication Route I (Fig. 1) of the UTAM surface patterning.11 The geometrical structures of the Au nanodots were tuned to optimize the enhancement of the SERS intensity. SERS spectra obtained from Au nanodot arrays with different heights reveal that the optimal height of the Au dots for SERS performance is 60 nm. This supplies an easy way to tune the SERS properties and hence to obtain SERS-active substrates with high sensitivity.

However, there are two challenging points preventing the UTAM patterning (e.g., Routes I–V in Fig. 1) in synthesizing regularly arrayed quantum-sized structures (<10–20 nm). First, the arrangement regularity of pores is poor when the pore diameter is smaller than 20 nm. Second, UTAMs that can be used for surface patterning should have pores with aspect ratio smaller than 10, e.g., the thickness of an UTAM with 20 nm-diameter pores should be smaller than 200 nm. However, UTAMs that are thinner than 200 nm are difficult to be prepared due to the large growth rate of UTAMs. Recently, we proposed an innovative route (Route VI) to prepare UTAMs with regularly arrayed pores in the quantum size range and successfully prepared ordered quantum dot arrays.12

A modulated anodization process was selected using sulfuric acid solutions with mixed solvents of glycol and water (volume ratio 3:2). Due to the low freezing point of glycol (modulator), the anodization was carried out at an extremely low temperature of −20 °C. This largely decreased the growth rate of UTAMs and an UTAM with a thickness of about 80 nm can be prepared (Fig. 2). Moreover, we used a well-controlled pore-opening process to prepare UTAMs with quantum-sized pores. There is an alumina barrier layer between the pore bottom and the Al foil of as-prepared UTAMs. The pore-opening (etching the barrier layer) was carried out using a 5 wt% H₃PO₄ solution. Fig. 3a–d shows the UTAM bottom surface in the pore-opening process with different etching times. Pores start to open with an etching time of 13 min, and pore-openings with diameters of about 5 nm were obtained with an etching time of 15 min. The diameter of pore-openings increases with the etching time, resulting in pore-openings of about 10 nm (18 min), 17 nm (24 min), 22 nm (30 min), and 27 nm (40 min). This means that the diameter of the pore-openings can be controlled based on the adjustment of the etching time. UTAMs with quantum-sized pore-openings can be used to fabricate ordered arrays of quantum dots (Fig. 3e). The large scale ordered arrays of quantum dots on substrates are promising candidate...
structures for new types of optoelectronic and display devices on the basis of the quantum confinement effect.

2.3 Nanopillar arrays

Besides the preparation of nanodots, UTAMs can be used to synthesize nanopillar arrays that are highly attractive in applications such as optical, magnetic, and electronic devices. Vapor-phase evaporation processes (a1 → a2 → a3 in Fig. 1) in growing nanodots cannot be used to prepare nanopillars directly on substrates. This is because the pore closure of the top porous layer will stop the growth of dots (aspect ratio < 3) before they become pillars (aspect ratio > 3). However, using deposition on the top of UTAMs or wet-chemical processes, nanopillar arrays can be prepared (Routes III and V in Fig. 1).

Highly ordered Au nanopillar arrays were prepared by evaporation on the top surface of UTAMs (Route III).26 The Au nanopillar arrays were released from the template and attached on a Si substrate (Fig. 4a) for SERS measurements. The SERS enhancement of Au nanopillar arrays is comparable with or better than that of the SERS substrates based on dispersed Au nanodots. Moreover, nanopillar arrays gave reproducible SERS signals in probing molecules (Fig. 4b), which makes it possible to realize highly reproducible SERS sensors for chemical and biological sensing.

A disadvantage of attached UTAMs is the poor adhesion of UTAMs to substrates. This could be solved by introducing a thin polymer layer between the UTAM and the substrate.27 Briefly, a thin layer of dihydroxy-terminated polystyrene or thiol-terminated polystyrene was grafted on a substrate. Such a grafted layer was then exposed to an ozone environment to enhance the wettability of UTAMs. Finally, UTAMs were transferred on surface-modified substrates. The good adhesion of UTAMs to substrates facilitates the fabrication of nanowire arrays on substrates. As an example, laterally long-range-ordered and free-standing poly(3-hexylthiophene) (P3HT) nanopillar arrays were synthesized on flexible polymer substrates (Fig. 5a and b).

Polymer plastic nanopillar arrays can be prepared by using anodic alumina membranes as molds.28 The alumina mold was placed on a photocurable prepolymer mixture layer dispersed on a glass substrate. The prepolymer mixture entered into the pores of templates due to capillary force (Route III). The polymerization process was triggered by UV light irradiation on the prepolymer. After etching away the mold, an ordered array of plastic nanopillars was obtained on the glass substrate, which is exactly a negative replica of the mold (Fig. 5c). These plastic nanopillar arrays are suitable to be used for quantitative optical microscopy. By using a simple solution wetting method and a subsequent annealing step, similar plastic nanopillars of semiconducting polymers were synthesized by Theato et al.29 These polymeric nanopillar arrays with large intersurface and good electrochemical properties have a potential application in building up ordered bulk-heterojunction solar cells.

Semiconductor, metal and oxide nanopillar arrays can be prepared by the fabrication Route V using connected UTAMs on substrates. Moskovits et al. prepared CdSe nanopillar arrays with an electrodeposition process.14 The length of the nanopillars can be controlled from about 50 to 500 nm with the same diameter of about 65 nm. It was found that the length and the crystallinity of the CdSe nanopillars have critical
influence on the electrochemical photovoltaic performance. The optimal structural parameter for the light power conversion efficiency is about 445 nm in length with an annealing treatment at 500 °C. Ag nanopillars arrays prepared using a similar process show tuneable optical transmission into a spectral regime with optimal characteristics, either selecting high absorptive or transmissive properties. Moreover, WO₂ nano-column arrays were synthesized at the bottom parts of a connected UTAM on a Si wafer. Starting with an Al/W/Ti trilayer on Si, a connected UTAM was prepared by anodization process. A following high-voltage anodization process gave rise to the formation of WO₃ nanopillars, and free-standing WO₃ nanopillar arrays were obtained after removing the alumina (Fig. 5d).

Anodization processes in preparing connected UTAMs sometimes generate thick barrier layers on substrates or corrosion of substrates. Hu et al. investigated the preparation of connected UTAMs on indium tin oxide (ITO) glasses with an adhesion layer of Ti. They found that a precise control of the thickness of the Ti layer within 0.2–0.5 nm is important in two aspects: first, to prevent the corrosion of the ITO film; second, to hinder the formation of a thick barrier layer between the UTAM and the ITO glass. This finding is useful in device applications where transparent ITO glass substrates are desirable such as in photonic devices.

2.4 Other UTAM-prepared surface nanostructures

In the aforementioned applications, UTAMs are mainly used as evaporation masks (Route I), replication molds (Route III), or substrates for growth (Route V). However, UTAMs have some other purposes in surface nano-patterning processes. Using UTAMs as supporting substrates (Route II), nanorings (Ag) and nanocone (Pd) arrays were prepared by sputtering. This method could be extended to other materials including oxides and semiconductors. Moreover, UTAMs are ideal etching masks in ionic and plasma etching processes (Route IV) to prepare regular arrays of nanoholes on substrates. Recently, InP and Si nanohole arrays were achieved through Ar⁺ ion plasma etching under the protection of UTAMs. UTAM-prepared metallic nanodots were also used as etching masks to prepared nanowires, such as large-area Si nanowire arrays prepared by metal-assisted chemical etching on Si wafers.

Besides the fabrication of nanowire arrays, nanotube arrays can be prepared by atomic layer deposition (ALD) using UTAMs as host templates. Based on the ALD-coating of TiO₂ inside and outside of UTAM pores, TiO₂ nanotube arrays were produced with high regularity (Fig. 6). Since ALD is a layer-by-layer coating process, the thickness of the TiO₂ nanotubes can be controlled precisely. These TiO₂ nanotube arrays were used to construct a planar optical waveguide sensor with sub-angstrom sensitivity.

3. PS template surface patterning

3.1 Concept of patterning processes using PS templates

Colloidal lithography is a general fabrication technique of surface patterning using monolayer colloidal particles as templates. Besides silica particle monolayers as a major colloidal lithographic template, monolayer PS sphere arrays provide another excellent template for colloidal surface patterning. Surface patterning technique using PS sphere templates will be introduced in this review article. PS sphere templates have been widely used in colloidal lithographic processes in fabricating surface patterns within the submicron and nanometre-sized range. The monolayer PS spheres can be prepared on flat substrates by different processes through self-assembly at water/air interface, drop casting, spin coating, and evaporation. Fig. 7 shows the main features of the PS surface patterning. Starting from monolayer PS spheres on substrates (the rectangle-surrounded part in Fig. 7), different kinds of surface patterns are prepared mainly by six fabrication processes (Processes I–VI). Using a
perpendicular evaporation on the PS sphere template, honeycomb arrays of nanodots are synthesized on substrates after removing the PS template (Process I: a1 → a2), which is a typical process of colloidal lithography. When the evaporation is carried out with a certain angle, arrays of crescent-shaped structures are obtained (Process II: b1 → b2). While the PS template is rotating at a certain rate in the evaporation process, nanoring arrays are fabricated (Process III: b1 → b3). Moreover, regular arrays of column structures can be prepared with a glancing angle deposition process (Process IV: c1 → c2). It is also feasible to cap the surface of PS spheres by metals or semiconductors using electrophoretic deposition processes. After removing the inner PS spheres, hollow sphere arrays are realized (Process V: d1 → d2). Moreover, nano-bowl arrays can be synthesized by infiltrating PS spheres in sol solutions or metallic salt aqueous solutions followed by the removal of the PS templates (Process VI: e1 → e2).

PS templates can be removed easily by organic solvents (e.g., toluene) or a burning process (e.g., 400 °C in air). The diameters of PS spheres can be adjusted within the range of about 50 nm to 4.5 μm while the spacing between the PS spheres is also controllable by plasma etching. This gives rise to tuneable structural parameters of PS-prepared surface patterns in similar size ranges. Due to the wide range of size controllability and the easy template-removing process, the PS surface patterning has high commercial relevance for device applications.

Based on intensive investigations of the PS surface patterning, the fabrication processes (Processes I–VI in Fig. 4) of PS sphere templates for surface patterning are well-established. PS spheres can be patterned into monolayer and multilayer packed templates. The monolayer PS template has attracted much more research interests due to its ability to prepare some unique surface structures, such as hollow spheres, nano-bowls, and nano-crescents.

3.2 Honeycomb arrays of nanodots

There is an aperture among every three adjacent PS spheres within the PS sphere arrays. These apertures form a periodic honeycomb array. Therefore, with a monolayer PS sphere template as a mask during evaporation processes, honeycomb arrays of periodic nanodot arrays can be fabricated on substrates after removing the PS templates (Process I). So far honeycomb arrays of different metallic nanodots were prepared. PS-prepared honeycomb arrays of Ni nanodots were used as catalysts to grow vertically arrayed carbon nanotubes (CNTs) (Fig. 8a).30 These CNT arrays reflect and diffract light, and they have a photonic band gap in the visible frequency range due to the honeycomb arrayed structure. The band gap location can be controlled by varying the structural parameters. Strong coherent oscillation signals from symmetric lattice vibrations were observed in Au honeycomb arrays,31 which is attributed to the large sensitivity of absorption spectra to the monodisperse size of Au nanodots.
the size and shape of the Au crescents and the mutual orientation of nano-crescents between the adjacent layers can be adjusted, which determines the polarization-dependent absorption of the array. It was found that the response of the plasmonic resonances of nano-crescents on the attachment of dielectric particles is very sensitive. This efficient method in fabricating 3D plasmon resonators with well-defined structures shows large potential for optical device applications.

3.4 Nanoring array

Using a so-called ‘tilted-angle-rotation thermal evaporation’ process (Process III), Giessen et al. prepared periodic metallic split-ring resonators with multiple structural controllability including the inner- and outer-ring size, the gap angle, as well as the thickness and periodicity of rings. A monolayer PS sphere template was annealed to reduce the aperture size between PS spheres and hence resulted in a more circular shape of PS spheres. In the following evaporation process of Au, the sample holder was tilted with an angle (15°–22°), and the PS template was rotating at a certain speed. Finally ordered arrays of Au split-rings were acquired after removing the PS spheres (Fig. 8c). Optical measurements of the surface plasmon resonance agreed well with simulations for the reflection spectra of the metallic split-ring arrays, which confirmed their excellent structure quality.

3.5 Nanopillar array

Glancing angle deposition (Process IV) was used to fabricate single- and multi-component nanopillar arrays of Cr and Si (Fig. 8d) on monolayer PS templates. This method is a thin-film deposition process in which the material was evaporated and impinged on the template from an oblique angle (e.g., 85°). Both Cr and Si single-component nanopillars perfectly replicated the hexagonal close-packed arrangement of the underlying PS spheres. More recently, hierarchical amorphous TiO2 nanopillar arrays were prepared by multidirectional glancing angle pulsed laser deposition on monolayer PS templates. Interestingly, the TiO2 nanopillar array can be transferred to other substrates. The TiO2 nanopillar array exhibits excellent superamphiphilicity without further UV irradiation and also shows enhanced photocatalytic activity. The combination of superamphiphilicity and photocatalytic activity is helpful in realizing excellent self-cleaning surfaces.

3.6 Hollow sphere array

Hollow sphere arrays have been intensively investigated due to their potential applications in surface-enhanced Raman scattering sensors, lithium-ion batteries, and solar cells. Recently, Si hollow sphere arrays were synthesized based on electrophoretic deposition of Si colloidal solutions (Process V). Si colloidal solutions prepared by laser ablation were used as the electrolyte of the electrophoretic process. Si nanoparticles are positively charged in the colloidal solution while PS spheres are weakly negatively charged. Thus the Si particles were attracted and moved to the surface of PS templates, attached on the surface, and finally covered the entire surface of the PS spheres. After removing the PS spheres,
micro/nanostructured Si hollow spheres were synthesized (Fig. 9a). Importantly, the structural parameters of the Si hollow spheres are controllable. Moreover, small holes were formed on the shells of the Si hollow spheres, and it is possible to use such hollow spheres as drug release or catalytic containers. This is a versatile way to fabricate micro- and nano-structured hollow spheres. Hollow spheres of metals (such as Ni and Ag)\textsuperscript{39,44} can be prepared through similar methods just by changing the colloidal solutions into metal salts for the electrodeposition process. Moreover, multi-component hollow spheres could be prepared by multi-step electrophoretic deposition processes.

3.7 Nanobowl array

Li et al. demonstrated a facile synthetic approach (Process VI) in fabricating Ag nano-bowl arrays based on monolayer PS templates.\textsuperscript{40} A silver acetate aqueous solution was first dipped on the surface of a PS template. A heat-treatment process removed the PS spheres and in the meantime the silver acetate decomposed to silver. The silver component preferentially adhered to the down-hemisphere surface of PS spheres, giving rise to the formation of Ag bowl-like structures (Fig. 9b). The bowl-like structures are composed of many tiny Ag nanoparticles. Due to the lotus leaf-like morphology with hierarchical micro/nanostructures, the film showed an extraordinary superhydrophobicity after chemical modification. Similar bowl-like TiO\textsubscript{2} structures but with smaller dimension (nano-metre-sized) were prepared through ALD processes.\textsuperscript{34} Ion milling was used to remove the top half of the TiO\textsubscript{2}-covered PS spheres. Subsequently, the other half of the PS spheres left on the substrate were dissolved by toluene, resulting in ordered arrays of TiO\textsubscript{2} nanobowls. Due to the smooth interior and exterior surfaces and the uniform sizes and thicknesses of these nanobowls, they could be used in solar cells, photocatalysis and photovoltaic devices.

4. BCP template surface nano-patterning

Compared to the UTAM and PS templates, the self-assembly of BCPs provides a parallel platform in producing some unique surface nanostructures,\textsuperscript{35–52} like lamellae, bicontinuous gyroids, concentric rings, and wave-like wires, which is determined by the composition and the chain architecture of BCPs. The BCP surface nano-patterning technique has been reviewed by Bang et al.\textsuperscript{4} Here we will discuss some recent progresses concerning the BCP template surface nano-patterning.

The self-assembly of BCPs has been widely investigated as alternative photoresist in photolithography. With this BCP lithographic method, smaller nanostructures can be prepared than those synthesized with conventional photolithography. BCP templates can also be adopted in “bottom-up” fabrication techniques towards surface nano-patterning.\textsuperscript{4} So far different surface structures have been fabricated by the BCP surface patterning technique, mainly including nano- and quantum-dots, nanowires, nanopores, nanotubes, cylinders, lamellae, bicontinuous gyroids, concentric rings, and wave-like wires. By changing the molecular weights of BCPs, the feature size of the BCP-prepared surface structures can be adjusted within a range of about 5–50 nm, which is not easily accessible by using other templates (e.g., PS). The behaviour of BCP thin films has attracted much interest, especially the controlling of the orientation and lateral ordering of nanostructures. There are two basic fabrication strategies of the BCP surface patterning: (1) position-selective deposition of materials on desired micro-domains; (2) transferring the BCP pattern to underlying substrates for direct formation of nanostructures or filling of the feature with functional materials. Fig. 10 gives some typical examples of BCP surface patterning. Desirable materials are deposited into the nanoscale grooves of BCP-prepared domains, such as random-oriented lamellar (a), cylindrical morphology (b), and 1D direct-assembled lamellar domains (c). Nanodots and nanowires are fabricated with the similar configurations of those of the BCP domains. Different ways can be used to remove BCP templates, such as chemical etching, burning or thermal treatment, and plasma rinsing.
Son et al. proposed a method\textsuperscript{45} to prepare densely packed arrays of semiconductor quantum dots on BCP (PS-\textit{b}-PMMA) surface patterns. Moreover, well-ordered 1D oriented arrays of quantum dots were patterned on surface-reconstructed BCP films by spin-coating processes. Importantly, PMMA blocks of the BCP films were located at the mesa phase of the patterns, leading to an inversion of the pattern height upon E-beam treatment. Thus the quantum dots can be placed either in the nano-grooves of the BCP domains or be selectively located in the PS mesa phase of the BCP patterns (Fig. 11). Dual-component semiconductor dots on BCP patterns were also fabricated using the method. Recently, by reducing metal salts in BCP templates, metallic single-component (Au) and dual-component (Au/Ag) nanodots were prepared.\textsuperscript{46} While single-component nanodots exhibit one localized surface plasmon (LSP) resonance, dual-component nanodots show two characteristic LSP resonances. These metallic nanodot surface patterns are promising plasmonic structures for enhancing electric fields.\textsuperscript{46,47}

\textbf{5. Device applications}

The time-saving and low-cost fabrication processes of template-based surface patterning techniques facilitate the real device applications of surface nanostructures in industry. Therefore, surface nano-patterning using templates is very important for a wide range of device application areas. Many template-based patterning processes can be used to realize large scale surface patterns with well-defined structures. Large pattern area and high throughput of surface patterns are highly desirable for many device applications while well-defined structures are the preconditions to achieve devices with controllable properties. Different surface patterns with device-related properties have been introduced in Sections 2–4 (e.g., Au nanopillar arrays with strong and reproducible SERS enhancement, Au nano-crescents with structure dependent plasmonic resonances). To demonstrate the importance of the template-based surface patterning in producing diverse devices, some typical device application results of template-prepared surface structures will be shown in this section.

Large-scale ordered arrays of multilayer nanodots of magnetic metals are very attractive to produce high-density magnetic storage devices. Using the UTAM surface patterning technique, ordered Fe/Pt multilayer nanodot arrays were fabricated with diameters of about 18 nm and periodicities of about 25 nm.\textsuperscript{53} The nanodots have a very high density of $10^{12}$ dots per in\textsuperscript{2}. Using a thermal annealing process, the disordered fcc phase of the nanodots converted to the $L1_0$ phase. The (001)-oriented Fe/Pt nanodot arrays show perpendicular magnetic anisotropy and large coercivity (Fig. 12). Using a similar method, Co/Pt magnetic nanostructure arrays were prepared on UTAM/Si substrates by magnetron sputtering.\textsuperscript{54} The Co/Pt structures were deposited on the top surfaces of UTAMs, forming a Co/Pt multilayer with ordered pores. Co/Pt nanodot arrays were also prepared over a very
large area (10 cm²). The average diameter and periodicity of these multilayer dot arrays are 25.3 nm and 43 nm, respectively. Both the Co/Pt multilayer pore structures and dot structures show strong perpendicular magnetic anisotropy. All these UTAM-prepared multilayer nanostructure arrays with perpendicular magnetic anisotropy are desirable structures for producing magnetic data storage media. Some non-metallic materials such as CoFe₂O₄ (CFO) also have large magnetocrystalline anisotropy and magnetostriction. Recently, CFO nanodot arrays on single-crystalline substrates of SrTiO₃ were fabricated using the UTAM surface patterning technique. The density of the nanodot arrays can be as high as 0.21 Terabits per in². Systematic investigations of the magnetic properties of the CFO nanodot arrays indicate that the dipole-dipole interaction between smaller nanodots is stronger than that between larger dots. The magnetization of larger dots can be switched to form a uniform out-of-plane magnetization by applying an external magnetic field perpendicular to the surface. The CFO nanodots show slim magnetization hysteresis loops and a unique temperature-dependent magnetic behaviour, which provides good possibilities to investigate oxide nanomagnets.

A recent work done by Choi et al. gives another excellent example for the device realization using template-prepared surface nanostructures. Large scale well-aligned nanowire arrays of Sn and MnO₂ were prepared using connected alumina membranes on Si wafers. The fabricated nanowires were integrated into lithium rechargeable microbatteries. Sn nanowire arrays served as the anode materials of the lithium microbatteries. A discharge capacity of about 400 mA h g⁻¹ was maintained after 15 cycles at a high discharge/charge rate of 4200 mA g⁻¹. MnO₂ nanowires were used as the cathode material for on-chip microbatteries. The discharge capacity of the MnO₂ nanorods is about 150 mA h g⁻¹ during a few cycles at a discharge/charge rate of 300 mA g⁻¹. This indicates that the template-prepared surface patterns are highly reliable, cost effective, and device-compatible for device production.

Template-prepared metal nanodot arrays are excellent structures for ultrahigh bit density memory devices. Hong and his coworkers demonstrate the realization of a metal nanodot memory using a BCP lift-off process. The fabricated metal nanodot memory device shows an ultrawide memory window of 15 V at ±18 V program/erase voltages, which has not been achieved before. Such a large window can be adopted for multilevel cell operations that alleviate the scaling issues in metal oxide memory devices. The low temperature process to form metal nanodots minimizes the possible reaction between the metal nanodots and tunnelling oxides that may deteriorate the device performance significantly. This metal nanodot memory with the simple and reliable BCP lift-off process opens new opportunities for terabit memory applications.

6. Summary and outlook

This article gives a general overview on the template-based surface nano-patterning techniques, focusing on three widely-used templates prepared by self-assembly processes: UTAMs, monolayer PS sphere arrays, and BCP patterns. Using these templates, surface patterns of different materials (metals, semiconductors, polymers, oxides) with diverse shapes and configurations (e.g., dot, rod, pillar, hole, ring, crescent, bowl, hollow sphere, cylinder, lamella, gyroid) were synthesized on substrates. The structural parameters of the template-prepared surface patterns largely depend on those of the templates. The feature size of the building blocks of these patterns can be adjusted from about 5 nm to about 4.5 μm, which covers the whole range from the quantum size to nanoscale, and then to microscale. The cost-effective and time-saving fabrication processes of template-based surface nano-patterning methods are highly desirable for industrial applications in fabricating different nano-devices, giving rise to broad applications of template-prepared surface nanostructures.

Future research of the template-based surface nano-patterning shall be more focused on device-related surface patterns with well-defined structures so as to realize nano-devices with tuneable properties and excellent performance. In addition, it is highly expected for the template surface patterning techniques to achieve more novel multifunctional and advanced composite surface structures with unique and interesting properties that are suitable for device integration.

Acknowledgements

Financial support from European Research Council Grant (ThreeDSurface), Volkswagen Stiftung, DFG (TRR61), and Shanghai Dong-Fang Scholarship is gratefully acknowledged.

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