Highly ordered nanostructures with tunable size, shape and properties: A new way to surface nano-patterning using ultra-thin alumina masks

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Abstract

Large-scale arrays of nanostructures on substrates, such as semiconductor or metal nano-particle arrays, have attracted considerable interest due to their unique physical properties and many potential applications in areas such as electronics, optoelectronics, sensing, high-density storage, and ultra-thin display devices. In the last two decades, the search for a highly efficient and low-cost nano-patterning method in fabricating ordered surface nanostructures with tunable dimensions and properties, has involved interdisciplinary and cross-disciplinary research and development with emerging technologies such as lithographic methods, self-assembly processes, and scanning probe techniques. Here, we review a new surface nano-patterning approach in fabricating ordered nano-structures, in which ultra-thin anodic alumina membranes are used as fabrication masks. Using the method, large-scale arrays of highly ordered nanostructures in the range of square centimeters can be fabricated on any substrate in a massive parallel way. The resulting nanostructures are characterized by highly defined and controllable size, shape, composition, and spacing of the nanostructures. Tuning of the properties of the arrayed nanostructures can be obtained by controlled adjustment of the structural parameters of the arrayed nanostructures. Compared to conventional lithographic methods, the present nano-patterning approach offers attractive advantages, such as large pattern area, high throughput, low equipment costs, and high flexibility and control options.
for ordered nanostructures with tunable properties. This new non-lithographic nano-patterning approach will be shown to be a general method in fabricating a wide range of ordered surface nanostructures with tunable and unique physical and chemical properties that could be used in the fabrication of nano-devices with high performance and controllability.

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1. Introduction

1.1. Surface nano-patterning

The emerging disciplines of nano-devices, including nano-electronics, nano-optoelectronics and sensing, require the development of surface nano-patterning techniques to obtain large-scale arrays of nanostructures (mostly nano-particles and nano-holes) on a given substrate, such as silicon (Si). In order to tailor the properties of the nanostructure arrays and the nano-devices, it is mandatory to fabricate ordered arrays of nanostructures with tunable size, shape, and spacing, using patterning techniques that are applicable to a wide range of materials. Moreover, it is technologically required to develop nano-patterning techniques that allow high throughput, large pattern area, and low equipment costs.

There are several nano-patterning methods for producing nanostructure arrays on substrates, including lithographic methods (such as electron-beam [1,2], ion-beam [3], and X-ray [4] lithography), self-assembly processes [5,6], scanning probe techniques [7], and methods that utilize diblock-copolymers [8–10]. Using these methods, many kinds of metal and semiconductor nanostructure arrays have been successfully fabricated on substrates. Electron beam lithography (EBL), as one of the most common lithographic methods, offers precise control over the size, shape, and spacing of the nanostructures. Self-assembly processes, which use the interaction of nano-particles to achieve the surface patterning, present efficient approaches in fabricating large areas of nano-particle arrays. The scanning probe microscopy (SPM) techniques are writing processes on substrates using both scanning tunneling microscopy (STM) and atomic force microscopy (AFM) with ultra-sharp nano-tips. The resolution that can be obtained with the SPM techniques can vary from the atomic-sized range to the micrometer-sized scale. The diblock-copolymer technique uses the interactions of two chemically distinct polymer chains to achieve ordered arrays of surface patterns with a size scale limited to chain lengths of the polymers. After the removal of one component polymer, an ordered porous nanostructure can be obtained on substrates, which can be used as a mask in fabricating nano-dots or nano-pores on substrates.

However, there are some fabrication and application restrictions for each of these methods. The EBL method has its inherent limitations, such as the limited pattern area, low throughput due to the long exposure time, high capital equipment costs and the restrictions that are coupled with the need to use resist materials. The self-assembly processes of nano-particles (including the diblock-copolymer approach), however, suffers from a rather poor control of spatial and size distribution of the resulting nanostructures, and it is only applicable to limited classes of materials. Moreover, byproducts are sometimes generated in the wet-chemical preparation of self-assembling particles, which makes it difficult to keep the substrate surface clean. The SPM techniques, due to their slow writing processes, cannot easily be adapted in fabricating large areas of nanostructured surfaces.
Based on these restrictions, the realization of highly ordered surface nano-patterning with a process characterized by flexibility, high throughput, low cost and high structural controllability presents an important and timely issue.

1.2. Anodic alumina nano-porous membranes

As a well-known nano-template, anodic porous alumina (Al₂O₃) membranes have been intensively studied over the last five decades [11–41]. Anodized from high-purity aluminum (Al) foils, porous alumina membranes have highly ordered nano-pore arrays with controllable structural parameters (Fig. 1a and b). Fig. 1d shows the configuration of the anodic alumina membranes. The structure of the anodic alumina membranes is a close-packed array of hexagonal cells, each containing a cylindrical central pore that is perpendicular to the surface of the underlying Al foil. The pores extend down to an alumina barrier layer between the pore bottom and the Al foil. This thin non-porous barrier layer has a hemispherical and scalloped geometry, and its thickness is half of the pore wall. For as-prepared alumina membranes, the pore diameter is between one third and half of the cell size. Using selected acid solutions to etch the pore walls and hence widening the pores, it is possible to adjust the pore diameters within the cell size. Fig. 1c shows a pore-widened alumina membrane with ultra-thin pore walls that originates from a long pore-widening process.

Fig. 1. Anodic alumina nano-porous membranes. Top view (a) and cross-sectional view (b) of a membrane with pore diameter and cell size of about 65 and 105 nm, respectively. (c) is the top view of a pore-widened membrane with ultra-thin pore walls. (d) is the configuration diagram of porous alumina membranes.
One of the most important advantages of the anodic alumina membranes is the tunable pore diameter and cell size [14–24]. The pore diameter of the alumina membranes (as-prepared without the pore-widening) is proportional to the anodization voltage and can be adjusted in the range of about 10–200 nm (the corresponding cell size is in the range of about 25–420 nm). Normally, three kinds of acid solutions are used for the anodization of the alumina membranes: sulfuric, oxalic, and phosphoric acid solutions. The sulfuric acid solution is suitable for the preparation of alumina membranes with small pores that are in the range of about 10–30 nm. The oxalic acid solution is suitable for the preparation of alumina membranes with medium-sized pores (about 30–80 nm) while the phosphoric acid solution is used for the preparation of large-pore membranes (larger than 80 nm). A good tuning of the pore diameter and cell size of the alumina membranes can be obtained for the small and medium-sized pore membranes. However, for alumina membranes with large pores (larger than about 100 nm), a narrow size distribution of pore diameter and cell size and regular arrangements of the pores cannot be obtained easily.

Mainly, the following chemical processes dominate the anodization of the alumina membranes [12,13,24]:

(1) \( \text{Al}^{3+} \) ions form at the metal/oxide interface and distribute in the oxide layer near the oxide/metal interface.

\[
\text{Al} = \text{Al}^{3+} + 3e
\]  

(2) The electrolysis of water (a water-splitting reaction) occurs at the pore bottom near the electrolyte/oxide interface [13,24]:

\[
2\text{H}_2\text{O} = 2\text{O}^2^- + 4\text{H}^+
\]  

(3) Due to the electric field, the \( \text{O}^2^- \) ions migrate within the barrier layer from the electrolyte/oxide interface to the oxide/metal interface, and react with the \( \text{Al}^{3+} \) ions there, forming \( \text{Al}_2\text{O}_3 \):

\[
2\text{Al}^{3+} + 3\text{O}^2^- = \text{Al}_2\text{O}_3
\]  

(4) There is an electric-field-enhanced oxide dissolution at the electrolyte/oxide interface:

\[
\text{Al}_2\text{O}_3 + 6\text{H}^+ = 2\text{Al}^{3+} \text{ (aq)} + 3\text{H}_2\text{O}
\]

In the anodization process of the porous alumina membranes, there is a balance between the electric-field-enhanced oxide dissolution at the electrolyte/oxide interface and the formation of oxide at the oxide/metal interface. This balance is crucial to the formation of the porous alumina membranes, since it makes the thickness of the barrier layer constant in the entire anodization process and hence allows steady-state pore propagation into the Al. The electric-field-enhanced oxide dissolution is the unique feature of the synthesis of the porous alumina that separates it from the barrier-type non-porous alumina anodized in neutral solutions.

The formation of the highly ordered hexagonal pore arrays of the alumina membranes is a self-organization process during the Al anodization [16–19]. It is suggested that the repulsive forces between the neighboring pores at the metal/oxide interface promote the
formation of ordered hexagonal pore arrays [18]. At the beginning of the anodization, pores nucleate at random positions on the Al foil surface. As the pores grow into the aluminum with the anodization process, the pores self-organize and hence the regularity of the pore arrays improves. Normally the regularity of the pores and pore arrangement increases with the anodization time, especially in the first several hours. Therefore, a conventional one-step anodization process with a relatively long anodization period will result in alumina membranes with disordered pores on the top and regular pores at the bottom of the membranes, i.e. alumina membranes with quite different pore regularity on the top and bottom of the membranes. A two-step anodization process that was proposed by Masuda and Satoh [16] successfully realized the fabrication of alumina membranes with regular pores throughout the whole membranes. In this process, after a long first anodization, the top-distorted first alumina layer is removed from the Al foil, leaving a highly ordered concave pattern on the surface of the Al foil. Then a second anodization is carried out on this surface-patterned Al foil, resulting in alumina membranes with regular pore arrays at both sides of the membranes.

To improve the pore regularity and the surface smoothness of the anodic alumina membranes, some pretreatments of the Al foils are necessary before the anodization, such as annealing and electropolishing. The annealing process of Al foils under vacuum conditions can remove the mechanical stresses in the Al foils and increases the grain size. This will facilitate the self-organization process of the pores in the following anodization. The electropolishing process (normally using mixture solutions of perchloric acid and ethanol) of Al foils can result in a smooth Al surface for the anodization. Experimental evidence suggests that the details of the surface topology of the Al foil, e.g. its surface roughness, are important for the regularity of the pore structure.

It should be mentioned that the pore arrangement of anodic porous alumina is usually far from an ideally packed hexagonal columnar array over a sizable region of, say, millimeter dimensions. The defect-free areas of the pore arrays are typically several square micrometers. The size of the defect-free areas increases with the anodization time. However, there seems to exist a limitation of this improvement, since so far the reported defect-free area of the self-organized alumina membranes is seldom larger than 10 μm, even with a quite long anodization period. The difficulty in obtaining long-range ordered pores of the self-organized alumina membranes limits their applications. In 1997, Masuda et al. proposed a so-called “pretexturing” process [22], which uses a single-crystal silicon carbide (SiC) mold to stamp an aluminum foil before anodization, and successfully realized alumina membranes with long-range ordered pore arrays of rather large defect-free areas (millimeter size).

The attractive advantages of the anodic alumina membranes, such as nanometer-sized channels, adjustable pore size and length, and ordered pore arrays, make the anodic alumina membrane an excellent template in fabricating ordered arrays of one-dimensional nanostructures [20–37], i.e. ordered nano-wire and nano-tube arrays. In the last two decades, many kinds of nano-wire and nano-tube arrays have been prepared using anodic alumina membranes as templates, which include metals [21,25–27,35], semiconductors [21,28–31], carbon [32–35], polymers [36], and other types of materials [37]. The nano-wire and nano-tube arrays can be released from the template by simply removing the alumina membranes using acid or alkali solutions. The size of the nano-wires and nano-tubes can be tuned with the pore adjustment of the alumina membranes. Besides the fabrication of one-dimensional nanostructures, anodic alumina membranes can be used as original in
fabricating metal and semiconductor replicated membranes [15,38–41], some of which have interesting physical and chemical properties.

Because most nano-wires and nano-tubes were prepared in alumina membranes with a barrier layer and aluminum layer at the backside, it is usually difficult to fabricate nano-wire or nano-tube arrays directly on substrates (such as Si), which greatly limits their applications in Si-based devices. Moreover, it is difficult to fabricate zero-dimensional nano-materials (such as nano-particles and nano-holes) on substrates directly using conventional alumina membranes. However, it would be very attractive, if the advantages of the anodic alumina membranes could be used in fabricating surface nanostructures of zero-dimensional materials on substrates.

1.3. The UTAM surface nano-patterning

Recently, a novel nano-patterning method, in which ultra-thin alumina membranes are used as deposition or etching masks, has successfully realized the fabrication of ordered arrays of surface nanostructures on substrates [16,42–129]. The ultra-thin alumina mask (UTAM), as a special type of the anodic alumina membranes, is a through-hole porous membrane with small thickness of about several hundred nanometers. The UTAMs can be placed or fabricated on substrates. A typical UTAM on Si is shown in Fig. 2a. The UTAM is quite thin with a thickness of about 350 nm. The pore regularity of the UTAM is very high. The area of the UTAM can be as large as several square centimeters. Because the pores of the UTAMs are short nano-channels with a small aspect ratio, UTAMs can be used as deposition or etching masks in fabricating ordered nano-particle or nano-hole arrays on almost any smooth substrate. Fig. 2b shows a typical sample of the structures of UTAMs and arrayed nano-particles on Si, where part of the UTAM has been removed. It can be seen that the pore regularity of the UTAM has been successfully transferred to the nano-particle arrays. Using etching processes, ordered nano-hole arrays can also be fabricated on substrates. This non-lithographic surface nano-patterning approach provides an efficient and low-cost alternative in fabricating large-scale ordered arrays of surface nanostructures.

Compared to other nano-patterning methods such as EBL, SPM, and self-assembly processes, this new nano-patterning method, the so-called UTAM nano-patterning approach, has some interesting and advantageous features that are closely related to the properties and applications of the ordered surface nanostructures:

1. Each nano-particle or nano-hole has almost identical size and spacing, and the size and spacing can be precisely controlled by changing the geometrical structure of the UTAMs. The pore diameter of UTAMs can be adjusted from about 10 to 200 nm, resulting in the size adjustment of nano-particles and nano-holes in the similar range. Moreover, it is also found that, by changing the pore aspect ratio of the UTAMs and the deposition process, the shape of arrayed nano-particles can be adjusted [48]. Such controllability of the size, spacing, and shape allows also tuning the properties of the ordered surface nanostructures.

2. From the pioneering work of Masuda and Satoh in 1996 [16], different types of materials have been fabricated into ordered nanostructures on substrates using the UTAM nano-patterning [42–129], including semiconductor, metal, and oxide nano-particle
arrays \[16,42–83,108–117\]; semiconductor, diamond, and metal nano-hole arrays \[60–64,83–107\]; and some other structures \[108–125,128,129\], such as nano-rings, nano-wires, nano-tubes, and nano-pores, which initiated from ordered nano-particle arrays or which were fabricated in a manner closely related to the UTAMs (please refer to Table 1). The broad range of materials demonstrates the general applicability of this surface nano-patterning approach in fabricating a wide range of ordered surface nanostructures.

3. Compared to conventional lithographic methods, this new nano-patterning approach possesses attractive advantages such as large pattern area (>1 cm²), high throughput, and low equipment costs. Moreover, the ultra-high density of the ordered nanostructures \[10^{10}–10^{12} \text{cm}^{-2}\] allows using these nanostructures in producing high-density data storage media, ultra-thin display devices, high-sensitivity sensors, and photonic crystal devices.
<table>
<thead>
<tr>
<th>Ref. no.</th>
<th>Mask</th>
<th>Nano-particles (substrates)</th>
<th>Nano-holes</th>
<th>Others</th>
<th>Fabrication method</th>
<th>Features and properties</th>
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<tbody>
<tr>
<td>[16]</td>
<td>A</td>
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<td></td>
<td></td>
<td>EBE</td>
<td>First nano-particle paper</td>
</tr>
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<td>[42]</td>
<td>A</td>
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<td></td>
<td>VE</td>
<td>Multiple nano-particles</td>
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<td>A</td>
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<td></td>
<td>MBE</td>
<td>Cathodoluminescence</td>
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<td></td>
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<td>Multi-layer nano-particles, PL</td>
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<td>[46]</td>
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<td></td>
<td>MBE, RIE</td>
<td>Multi-layer nano-particles, PL</td>
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<td>EBE</td>
<td>Magnetic hysteresis</td>
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<td>TE, EBE</td>
<td>Size and shape tuning</td>
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<td>EBE</td>
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<td>A</td>
<td>Ag, Ni, ZnO, Si:Er (Si)</td>
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<td></td>
<td>PLD</td>
<td>PL, XPS, plasma plumes</td>
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<tr>
<td>[57]</td>
<td>A</td>
<td>ZnO (Si)</td>
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<td></td>
<td>EBE</td>
<td>PL and micro-Raman</td>
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<td>[58,59]</td>
<td>A</td>
<td>Au (glass) in liquids and gas</td>
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<td>C</td>
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<td>[61,62]</td>
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<td>Au, InAs</td>
<td>GaAs</td>
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<td>RIE, VE, MBE</td>
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<td>Au, Ni, Co, Fe, Si (Si, GaAs)</td>
<td>GaAs, GaN</td>
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<td>EBE, RIE</td>
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<td>[65]</td>
<td>A</td>
<td>Si (Si)</td>
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<td>TiO₂ (Ti and TiN/substrate)</td>
<td>TiO₂ nano-tips</td>
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<td>Anodization</td>
<td>Nano-scale field emission arrays</td>
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<th>Fabrication method</th>
<th>Features and properties</th>
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<td>AFM pretexturing, $C$–$V$</td>
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<td></td>
<td>PE</td>
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<td>A</td>
<td>ZnTe</td>
<td></td>
<td></td>
<td>RIE</td>
<td></td>
</tr>
<tr>
<td>[104]</td>
<td>A</td>
<td>Si/Si$_3$N$_4$</td>
<td>Molecules in holes</td>
<td>RIE, wet etch</td>
<td>Electrolyte–molecule–silicon</td>
<td></td>
</tr>
<tr>
<td>[105,106]</td>
<td>C</td>
<td>Al</td>
<td></td>
<td></td>
<td>PE and IM</td>
<td></td>
</tr>
<tr>
<td>[107]</td>
<td>C</td>
<td>Si nano-pillars</td>
<td></td>
<td></td>
<td>RIE</td>
<td>Pretexturing (nano-imprinting)</td>
</tr>
<tr>
<td>[108,109]</td>
<td>C</td>
<td>SiO$_2$ islands (Si)</td>
<td></td>
<td>Cu$_2$O NWs, CNTs</td>
<td>ECD, CVD</td>
<td>NWs and NTs on SiO$_2$ islands</td>
</tr>
<tr>
<td>[110]</td>
<td>C</td>
<td>Cu (Si)</td>
<td>Cu NWs</td>
<td></td>
<td>ELP</td>
<td></td>
</tr>
<tr>
<td>[111]</td>
<td>C</td>
<td>Co (Nb/Si)</td>
<td>CNTs</td>
<td></td>
<td>ECD</td>
<td></td>
</tr>
<tr>
<td>[112]</td>
<td>A</td>
<td>Ni (Si)</td>
<td>CNTs</td>
<td></td>
<td>TE</td>
<td></td>
</tr>
<tr>
<td>[113]</td>
<td>A</td>
<td>Au (GaAs)</td>
<td>GaAs NWs</td>
<td></td>
<td>EBE and MBE</td>
<td></td>
</tr>
<tr>
<td>Reference</td>
<td>Mask</td>
<td>Material System</td>
<td>Feature</td>
<td>Fabrication Method</td>
<td>Other Notes</td>
<td></td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>-----------------</td>
<td>---------</td>
<td>--------------------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>[114]</td>
<td>C</td>
<td>Au (Si, Au/Ti/Si)</td>
<td>Au NWs</td>
<td>VE and ECD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[115]</td>
<td>C</td>
<td>Ni (Si)</td>
<td>Ni NWs</td>
<td>ECD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[116]</td>
<td>A</td>
<td>Au (GaN)</td>
<td>ZnO NWs</td>
<td>EBE and VLS</td>
<td>PL</td>
<td></td>
</tr>
<tr>
<td>[117]</td>
<td>C</td>
<td>InGaN (GaN)</td>
<td>InGaN NRs</td>
<td>MOCVD</td>
<td>PL</td>
<td></td>
</tr>
<tr>
<td>[118,119]</td>
<td>A</td>
<td>Au, Ni, Si NRs</td>
<td>SP and TE</td>
<td>Spin waves in Ni nano-rings</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[120]</td>
<td>A</td>
<td>Au (Ti/Si)</td>
<td>Au NTs</td>
<td>SP and TE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[121]</td>
<td>C</td>
<td>(Si)</td>
<td>TiO₂ NTs</td>
<td>ALD</td>
<td>Pretexturing, absorption-spectra</td>
<td></td>
</tr>
<tr>
<td>[122]</td>
<td>C</td>
<td>(Si)</td>
<td>Ag NWs</td>
<td>ECD</td>
<td>Pretexturing</td>
<td></td>
</tr>
<tr>
<td>[123]</td>
<td>C</td>
<td>(W/Si, Pt/MgO)</td>
<td>CoPt₅L₁₀ columns</td>
<td>ECD</td>
<td>Magnetic measurement</td>
<td></td>
</tr>
<tr>
<td>[124,125]</td>
<td>C</td>
<td>(Si, glass)</td>
<td>Bi, BiTe, Au NWs</td>
<td>ECD</td>
<td>Barrier layer structures</td>
<td></td>
</tr>
<tr>
<td>[126,127]</td>
<td></td>
<td>Au (Au nano-islands)</td>
<td>Au NWs</td>
<td>Self-assembly nano-dot/molecule/nano-island</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[128]</td>
<td>A</td>
<td>ZnO nano-pores</td>
<td>SP</td>
<td>Multilayer ZnO nano-pores</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Abbreviation in the table:
1. Mask: A = attached UTAMs; C = connected UTAMs.
2. Others: CNT = carbon nano-tube; NT = nano-tube; NP = nano-pillar; NR = nano-ring; NS = nano-sphere.
3. Fabrication methods: EBE = E-beam evaporation; VE = vacuum evaporation; TE = thermal evaporation; SP = sputtering; MBE = molecular beam epitaxy; PLD = pulsed laser deposition; IM = ion milling; RIE = reactive ion etching; PE = plasma etching; II = ion implantation; ELP = electroless plating; ECD = electrochemical deposition; VLS = vapor–liquid–solid; MOCVD = metalorganic chemical vapor deposition; FAB = fast atom beam.
4. Because the ordered nanostructures that are fabricated using the UTAM nano-patterning approach are mostly prepared on device-related semiconductor substrates, such as Si, GaAs, and GaN, the nanostructures are suitable to be applied in the fabrication of semiconductor devices.

All the above-mentioned research achievements concerning the UTAM nano-patterning approach open a new and promising research field in the research discipline of ordered nanostructures and nano-devices. The advantages of the UTAM nano-patterning approach, such as the tunable structural parameters and large pattern area, high throughput and low equipment costs of the fabrication processes, general applicability in fabricating ordered nanostructures, tuning of the properties of the ordered nanostructures, make the technique quite suitable to fabricate ordered surface nanostructures with tunable properties and hence nano-devices with good performance.

1.4. Scope of the paper

This contribution gives a systematic overview on the fast growing research field of the UTAM nano-patterning, which includes the fabrication processes, the associated properties, and the applications of the ordered surface nanostructures. Because this paper only focuses on the research concerning the use of UTAMs in fabricating surface nanostructures, research results on nano-fabrication using conventional “thick” alumina membranes are not included, but are the subject of a current review by Seal et al. [130].

We first give a detailed description of the fabrication processes of the UTAM nano-patterning and the specific features of two kinds of basic UTAMs. Then the research progress concerning ordered arrays of nano-particles, nano-holes, and other nanostructures are introduced separately. Besides the introduction of the fabrication processes, we will focus on the structure-related properties and the application aspects of the ordered surface nanostructures.

2. Technological processes of the UTAM surface nano-patterning

The details of the nanostructures (particle, holes and others) that are fabricated using the UTAM nano-patterning, which includes the materials, substrates, fabrication method (deposition, etching, and others), and the features and properties of the nanostructures are summarized in Table 1.

2.1. General fabrication processes

Fig. 3 shows the schematic outline of the general fabrication process for nano-particles and nano-holes. First, an UTAM is fabricated on the surface of a substrate (Fig. 3a). Then nano-particles and nano-holes are fabricated using deposition (Fig. 3b1) and etching methods (Fig. 3b2), respectively. Finally the UTAM is removed, leaving highly ordered nano-particle (Fig. 3c1) or nano-hole (Fig. 3c2) arrays on substrates. Fig. 3d1 and d2 are examples of highly ordered arrays of nano-particles (Pd) and nano-holes on Si substrates, which were fabricated using similar UTAMs. Both the arrayed nano-particles and the nano-holes inherit the regularity of the UTAMs.
Most of the deposition methods in fabricating nano-particle arrays are vapor-phase deposition processes (Table 1), which include thermal and E-beam evaporation (vacuum evaporation), sputtering, molecular-beam epitaxy (MBE), pulsed laser deposition (PLD), and chemical vapor deposition (CVD). In the case of using connected UTAMs (refer to Section 2.2 for the details concerning the connected UTAM), wet chemical approaches such as electrochemical and electroless deposition can also be used in fabricating ordered nano-particles on substrates. Besides the nano-particles at the bottom of the
nano-channels, there is a sieve-like layer formed at the top of the pore walls of the UTAM (Figs. 2b and 3b1) when using vapor-phase deposition approaches. At the beginning of the deposition, the pores of this top layer have a diameter similar to that of the pores of UTAMs. As the deposition progresses, the pores of the top layer shrink continuously and finally results in the closure of the pores and the termination of the nano-particle growth. This is the closure effect in the growth process of the nano-particles using vapor-phase deposition.

The etching processes used to excavate holes in substrates include reactive ion etching (RIE), plasma etching (PE), and fast atom beam (FAB) etching processes (Table 1). Ion implantation followed by a chemical etching process is also available in fabricating nano-holes on substrates [98].

2.2. Two types of UTAMs: attached UTAM and connected UTAM

Two different types of UTAMs exist: attached UTAM and connected UTAM. Attached UTAMs are first fabricated on Al foils, and then they are detached from the foils and attached to the surface of the chosen substrate. Connected UTAMs are prepared directly on substrates and the UTAMs are anodized from Al films that were deposited on the substrate.

The fabrication process of the attached UTAM is outlined in Fig. 4. The UTAMs are prepared in a two-step anodization process (Fig. 4a–d) [16,48]. High-purity (99.999%) aluminum foil is used as the starting material (Fig. 4a). After the first anodization step (Fig. 4b), the anodic oxide layer is removed in a mixture solution of H₃PO₄ (6 wt.%) and H₂CrO₄ (1.8 wt.%) at 60 °C (Fig. 4c). This specimen is anodized again for a short time (normally several minutes), resulting in an ultra-thin alumina layer (Fig. 4d). A polymer (e.g. PMMA) layer is then fabricated on the top of the ultra-thin alumina layer and it will be used as a supporting layer for the UTAM (Fig. 4e). After that, the Al layer and the barrier layer at the back side are removed, forming a through-hole UTAM (Fig. 4f). Then the UTAM/polymer is mounted on the substrate (Fig. 4g). Finally, the polymer layer is removed, leaving the attached UTAM on the substrate (Fig. 4h). Normally the thickness of the attached UTAMs is in the range of several hundred nanometers and it is usually

![Fig. 4. Schematic outline of the fabrication processes of attached UTAMs. (a) Aluminum foil; (b) first anodization; (c) removal of alumina; (d) second anodization; (e) polymerization of MMA; (f) removal of Al layer and barrier layer; (g) pore widening and mount onto substrate; (h) removal of PMMA layer.](image)
smaller than 1 μm. A short channel of the UTAM can facilitate the evaporated material or the etchant to reach the surface of the substrates.

Fig. 5 indicates the fabrication process of the connected UTAMs. First, a high-purity Al layer is deposited on the surface of the substrate using thermal or E-beam evaporation (Fig. 5a and b). A two-step anodization process similar to that of the attached UTAMs is used to fabricate the connected UTAMs on substrates (Fig. 5b–e). The first anodization is carried out till a thin Al layer is left on substrates (Fig. 5c), and the second anodization will consume all the remaining Al (Fig. 5d and e). Finally, a penetrating process (details of the penetrating process can be found in Section 2.3.3) removes the barrier layer and results in connected UTAMs on substrates with through pores (Fig. 5f). For the connected UTAMs used in the vapor-phase deposition for nano-particles and the etching process for the nano-holes, the thickness of the UTAM should be small (similar to the case of the attached UTAMs). However, when the connected UTAMs are used in wet-chemical processes in fabricating nano-particle arrays on substrates, there is no strict limitation for the thickness of the UTAMs.

Fig. 6 shows an attached UTAM (a) and a connected UTAM (b) on substrates.

2.3. Features and advantages of both UTAMs concerning the fabrication process

Attached UTAMs and connected UTAMs each have their own specific features and advantages. Both of them are widely used in the UTAM nano-patterning process. In the following a comparison is made between the attached UTAM and the connected UTAM regarding the regularity of the pore arrays and the capability in fabricating ordered surface nanostructures.

2.3.1. Regularity

Because attached UTAMs are fabricated on Al foils and the thickness of the foil is usually in the range of hundreds of micrometers, a long first anodization period (usually 10 h or more), which is a precondition to obtain highly regular pore arrays, is always used in fabricating attached UTAMs. For example, the attached UTAMs in Figs. 2a and 6a have
A long first anodization at 40 V in 0.3 M oxalic acid solution at 17 °C for 10 h. The thickness of the consumed Al in the first anodization is about 80 μm.

For connected UTAMs, because the thicknesses of the evaporated Al layers on substrates are usually limited (below 10 μm), the regularity of the pore arrays of the connected UTAMs are not as high as that of the attached UTAMs. The Al layers on substrates are fabricated using vacuum evaporation processes, and the evaporation of a relatively thick Al foil (i.e. larger than 20 μm) is usually quite time-consuming. The connected UTAM in Fig. 6b is fabricated from a 4 μm-thick evaporated Al layer. Clearly it can be seen that the regularity of this connected UTAM is far worse than that of the attached UTAM in Fig. 6a.

Table 2 indicates the relationship between the thickness of the evaporated Al layer and the pore regularity of the connected UTAM (and the resulting nanostructures). Fig. 7
Table 2
Relationship between the thickness of evaporated Al layer of the connected UTAMs and the pore regularity of UTAM

<table>
<thead>
<tr>
<th>Ref. nos.</th>
<th>[75,77]</th>
<th>[67,69,73,75,108,109]</th>
<th>[71,72,100–103,114,117]</th>
<th>[78,85,88]</th>
<th>[76]</th>
<th>[124]</th>
<th>[80,89,110]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness of the evaporated Al layer (μm)</td>
<td>0.3</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>5</td>
<td>6–12</td>
<td>20</td>
</tr>
<tr>
<td>Pore regularity of UTAM (or the resulting nanostructures)</td>
<td>Poor</td>
<td>Poor</td>
<td>Fair</td>
<td>Fair</td>
<td>Fair</td>
<td>Fair</td>
<td>Good</td>
</tr>
</tbody>
</table>
shows an example of the improvement of the pore regularity of the connected UTAMs with the increment of the thickness of the Al layer. Most of the connected UTAMs in Table 2 and Fig. 7 were fabricated under similar anodization condition (40 V in 0.3 M oxalic acid solution). Under this condition, there is almost no regularity of the pores of the connected UTAMs fabricated on Al layers with thickness smaller than 1 μm (e.g. 0.5 μm in Fig. 7a). The regularity of the UTAMs increases but still is not high when the thickness of the Al layer increases to 1 μm (Fig. 7b) and even to 6–12 μm (Fig. 7c). A relatively high regularity of the UTAMs can only be obtained when the thickness of the Al layer increases to 20 μm (Fig. 7d).

To overcome the thickness limitation of the evaporated Al foil in improving the regularity, a pretexturing process (nano-imprinting), which uses SiC or Si₃N₄ molds to stamp the evaporated Al before anodization, was used and it successfully fabricated highly regular connected UTAMs that are anodized from thin evaporated Al layers [60,122]. There are ordered convex patterns on the surface of the molds. After the pretexturing process, ordered arrays of shallow concave imprints are formed on the surface of the Al layer.

Fig. 7. An example of the dependence of the pore regularity of connected UTAMs on the thickness of the deposited Al layer on substrates. The connected UTAMs in (a), (b), (c), and (d) are fabricated from Al layers with thickness of about 0.5, 1, 6–12, and 20 μm, respectively. Images in (a), (b), (c), and (d) are reproduced with permission from Refs. [108] (copyright 2004, Elsevier), [100] (copyright 2004, American Institute of Physics), [124] (copyright 2003, Wiley-VCH), and [89] (copyright 2001, American Vacuum Society), respectively.
In the following anodization process, these concave imprints will serve as nucleation points for the formation of alumina nano-pores. Fig. 8 shows a connected UTAM that was fabricated from a 0.8 μm-thick Al evaporated layer using the pretexturing process [60]. The pore regularity is very high and is in fact much better than that of the UTAMs fabricated from the Al layer of similar thickness but without the pretexturing process (Fig. 7a and b).

The molds for the pretexturing process are patterned using the EBL method, and the fabrication of large-area patterned molds is time-consuming and expensive. Sander et al. proposed an alternative pretexturing process in fabricating connected UTAM with high pore regularity [121]. In the pretexturing process, instead of using an expensive lithographically patterned mold, an anodic alumina membrane that was created from Al foil using the two-step anodization process was used as the imprinting mold. The Al on the backside of the alumina membrane was removed. To imprint the Al film, the alumina mold was placed with the bottom surface of the barrier layer (with ordered convex pattern) on the Al film. While this method does not require a lithographically patterned mold and can be used to imprint relatively large areas (~1 cm²), the alumina mold is rather fragile and cannot be reused. Also, the regularity of the UTAMs is not as high as that of the UTAMs patterned using the EBL-made molds.

2.3.2. Capability and versatility in fabricating ordered surface nanostructures

Because attached UTAMs are maintained on substrates via a weak Van der Waals surface attachment (e.g. a quick drying process of acetone), the UTAMs are not in good connection with the underlying substrates. A subsequent wet-chemical process may cause the detachment of the UTAM from the substrate. Therefore, the attached UTAM can only be used in vapor-phase deposition processes for fabricating ordered nano-particles or nano-holes. For connected UTAMs, due to the masks remaining in intimate connection with the substrate, they can be used in both vapor-phase deposition and wet-chemical processes to direct the deposition of nano-particles onto the underlying substrates. This is an important advantage of the connected UTAMs compared to the attached UTAMs. Moreover, also
due to the good connection between the connected UTAM and the underlying substrates, it is possible to carry out post-deposition treatments of the UTAM/particle/substrate (or UTAM/hole/substrate) structure, such as the removal of the top layer on the UTAMs, or the electrochemical deposition of particles into the etched holes. Therefore, the connected UTAM offer a larger versatility in fabricating different ordered surface nanostructures than the attached UTAM and, especially in combination with the imprint technology, nanostructuring with connected UTAMs offer the combined advantages of high regularity, high throughput and high versatility.

2.3.3. Fabrication of connected UTAMs on substrates with through holes (penetrating)

A key point in using the connected UTAM to fabricate nano-particles on substrates is how to penetrate the barrier layer and thus obtaining through holes so that the deposited materials (either using vapor-phase or wet-chemical processes) can pass through the channels of the UTAM and reach the surface of the substrates. The following is a detailed discussion on how to penetrate the barrier layer of the connected UTAM.

2.3.3.1. Arched barrier layer structures of the connected UTAM on substrates. It is found that the oxide barrier layer of the connected UTAM has a unique arched (inverted) structure with a void beneath the barrier layer (Fig. 9), both in the case on Si [85–87,124] and other substrates [88]. This is quite different from the hemispherical barrier layer of the anodic alumina membranes fabricated on Al foils.

Fig. 10 gives the schematic outline of the formation of the arched barrier layer. When the oxide/Al interface reaches the surface of the substrate, the barrier layer is still hemispherical and Al pyramids form between the pore bottoms (Fig. 10a). With further anodization, the Al pyramids keep on being converted into alumina. This will cause additional electric-field-enhanced dissolution of alumina at the sides of the pore bottom and almost no dissolution in the base of the pore bottom, leading to the gradual formation of a rectangular pore bottom (Fig. 10b) and further tiny oblique pores on the wall (Fig. 10c). In the meantime, due to the hydrogen ion-assisted [86] or electric-field-enhanced dissolution [85] of the oxide at the oxide/substrate interface, a void forms beneath the barrier layer.
(Fig. 10b) and continues growing with further oxide dissolution. Finally, an arched barrier layer forms through the combination of the oblique pores and the enlarged void (Fig. 10c).

2.3.3.2. **Penetrating the barrier layer.** The arched barrier layer is thinner than the hemispherical barrier layer, thus it is possible to remove the arched barrier layer using a chemical etching process [60,100,114]. However, the chemical etching process of the barrier layer is always accompanied by a pore-widening process. A complete removal of the barrier layer may cause large pores with very thin pore walls which is sometimes undesirable. Another possible way to remove the arched barrier layer is to continue the anodization using a ramped voltage after the formation of the arched barrier layer [87]. However, this procedure will etch the substrate such as Si, forming silicon oxide (SiO₂), or metal oxides in the case of Si/metal substrates (Si coated with a metal layer).

A well-controlled thinning process proposed by Nielsch et al. [25] can be used to penetrate the barrier layer of the connected UTAMs (Fig. 11) [122,131]. As known, the thickness of the barrier layer is proportional to the applied anodization voltage. When the oxide/Al interface nearly reaches the substrate, the applied anodization voltage is stepwise reduced. During the voltage reduction, the pores split into small pores (Fig. 11b) and finally a “dendritic” pore structure forms (Fig. 11c). During this process, the thickness of the barrier layer decreases finally to zero. This is a direct approach in fabricating through-hole UTAMs on substrates. However, the undesirable dendritic structure at the pore/substrate interface will limit the application of the UTAM/substrate in fabricating surface nanostructures where the connection part to the substrate is crucial to the properties of the surface nanostructures.

Recently, Rabin et al. proposed a penetrating process and successfully obtained through-hole connected UTAMs on Ti-coated Si substrates [124]. The removal of the barrier layer was achieved by applying a reversed bias on the sample in KCl solution for a few minutes after the anodization process. Moreover, Tian et al. indicate that the penetrating
process can be completed in situ in one step by reversing the polarity of the anodization voltage in the same solution of the anodization [125].

2.3.3.3. Connected UTAMs on metal-coated Si substrates. The connected UTAM on Si substrate is a structure that is well-suited for fabricating ordered nano-particle and nano-wire arrays using electrochemical deposition. However, Si is not a good electrode for the electrochemical deposition. Moreover, the adhesion between the evaporated Al and the Si substrate sometimes is not sufficient in the electrochemical plating solutions. Therefore, thin metal layers were usually deposited between the Al and the Si substrate. These metal layers act as electrode in the following electrochemical plating process and also improve the adhesion of the Al (and consequently of the UTAM) to the Si substrate. Actually, most of the connected UTAMs for electrochemical deposition are fabricated on metal-coated Si.

Ta, Ti, and W could be selected as the inter-layer between Al and Si. Using these metals, especially Ti, the adhesion of the Al (and the connected UTAM) to the substrate can be largely enhanced. However, after full anodization of the Al, the metal layer was also anodized into metal oxides, such as Ta$_2$O$_5$ [71–75], TiO$_2$ [76–78], and WO$_x$ [123]. These oxides are poor electrodes for electrochemical deposition.

Au and Pt are excellent metals as electrochemical electrodes in UTAM/metal/Si structures. However, both of them are not good adhesion promoters. The UTAMs fabricated on Au or Pt coated Si have a poor adhesion to the substrates.

It is found recently that a Ti/Pt binary metal layer on Si substrates (Al/Ti/Pt/Si), is an excellent interlayer between Al and Si. Pt provides a good electrochemical electrode while Ti enhances the adhesion of Al to Si. A key factor of the application of this structure in electrochemical deposition is how to penetrate the Ti layer after the penetration of the oxide barrier layer, forming through holes on Pt-coated Si. Several efforts have been made recently and the penetration of the Ti layer was successfully achieved. It is found by Yasui et al. [123] that the oxide barrier layer and the Ti layer can be removed by a pore-widening process using acid solutions. Another penetrating process, which was proposed by Crouse et al., can directly remove the oxide barrier and Ti layer using a ramped voltage at the end of the anodization [87].

Finally, it should be mentioned that it is possible to deposit metal into pores with barrier layers. Wu et al. demonstrated an interesting process to electrochemically deposit Ni nano-particles and nano-wires into the pores of connected UTAMs with barrier layers [115]. This is accomplished by using a negatively charged UTAM as the cathode in the electro-deposition of Ni. However, to realize the application of ordered nanostructures on Si-based devices, an oxide barrier layer between the obtained nanostructure and the Si substrate is usually undesirable.

2.4. Some special fabrication routes

Besides the above-mentioned general fabrication processes for the preparation of nano-particle and nano-hole arrays, there are some other special or modified routes in fabricating ordered surface nanostructures.

Liang et al. [63] proposed an approach to fabricate ordered nano-particle arrays (Fig. 12) using the combination of particle deposition and etching processes. First, metal or metal oxide nano-particle arrays are fabricated on the desirable substrates (Fig. 12a)
using the UTAM nano-patterning approach. Afterwards, plasma etching is carried out using the nano-particles as etching caps or masks (Fig. 12b). Because the etching rate of the particle-capped area is smaller than that in the non-capped area, nano-particles are finally obtained on substrates. At the same time, the cap nano-particles have been (or almost) etched away (Fig. 12c). So far Si [63,65,68,69] and SiO₂ [67] nano-particles were successfully fabricated on substrates using Ni and Ta₂O₅ nano-particle caps. Because the fabricated nano-particles are actually part of the substrate, they have the same crystal structures as that of the substrate, and of course a perfect connection to the substrate.

Using a tilting evaporation process (Fig. 13), multiphase metal nano-particles can be fabricated on substrates [42]. Multiphase nano-particles are composed of two deposits

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![Fig. 12](image1.png)  
Fig. 12. Schematic outline of the fabrication processes of substrate-connected nano-particles using UTAM-fabricated nano-particles as etching caps. (a) Nanoparticles fabricated using UTAM; (b) etching process; (c) nanoparticles.

![Fig. 13](image2.png)  
Fig. 13. Fabrication of multiple nano-particles on substrates (reproduced from [42] with permission, copyright 2000, Wiley-VCH Verlag GmbH). (a)–(d) Schematic outline of the fabrication process; (e) Au/Au multiple nano-particles; (f) Au/Ag multiple nano-particles.
of identical (e.g. Au/Au particles in Fig. 13e) or different metals (e.g. Au/Ag particles in Fig. 13f). Each material is deposited in a small off-normal incident angle of about 5° (Fig. 13b and c). Multiphase nano-particles which compose of three deposits can also be fabricated using this process [42]. Moreover, by depositing different materials layer by layer, multi-layer nano-particles can also be fabricated on substrates [45].

Another interesting surface nanostructure that can be fabricated using UTAM nano-patterning is presented by nano-particles confined in nano-holes. The fabrication process includes first the etching of nano-holes on substrates and then the deposition of nano-particles into the holes. Au [61] and InAs [62] nano-particles have been fabricated into the nano-holes etched in GaAs substrates. It is found that InAs nano-particles were epitaxially grown in the GaAs nano-holes, and each GaAs nano-hole confined only one InAs nano-particle.

A widely used process in fabricating oxide nano-particle arrays on substrates using UTAM is to fully anodize Al/metal/substrates or Al/Si. Using this method, ordered arrays of metal oxides nano-particles were obtained on substrates, such as TaO_x [71–75], NbO_x [70,71], TiO_2 [76–78], WO_3 [123], and SiO_2 [79,108,109]. This process will be introduced in detail in Section 3.3.5.

Other processes for fabricating nano-particle arrays include e.g. the fabrication of Al pyramid arrays. As mentioned above, there is a pyramid-like Al particle formed (Fig. 10) when the oxide/Al interface reaches the substrate in the anodization process of the connected UTAM. After etching away the oxide layer, Al pyramid arrays can be obtained on substrates [80,81]. It is also possible to adjust the size of the Al pyramids by controlling the final anodization period since the size of Al pyramids decreases with the anodization duration (Fig. 10a and b).

For the fabrication of UTAMs, recently Toh et al. fabricated a free-standing UTAM that is peripherally supported on a Si substrate [127]. First, sub-millimeter holes were produced on Si substrates (with thin SiN layers on both surfaces of Si) using a photolithography process and an anisotropic chemical etching process (Fig. 14). Then an Al layer was sputtered on the top, followed with the anodization process. SiN and the barrier layer were finally removed using ion-milling, resulting in a free-standing UTAM on a Si substrate. This free-standing UTAM, due to the support of the substrate, may have a good operation capability for fabricating ordered nanostructures.

3. Highly ordered nano-particle arrays on substrates

Nanometer-sized particles are one of the main building blocks of nano-devices. In the application of nano-particles such as in the fields of optical and electronic devices, it is usu-
ally desirable to fabricate ordered arrays of nano-particles on substrates to improve the controllability and performance of the nano-devices. The UTAM nano-patterning has been recognized as a suitable method for fabricating ordered nano-particle arrays on substrates with controllable structural parameters and tunable properties. In this chapter, tuning of the size, shape, and spacing of arrayed nano-particles are introduced first. Then the research results of metal and semiconductor nano-particle arrays are reviewed separately. The propensity for tuning the properties of the materials by suitable adjustment of structure and/or morphology of the nano-particles presents the underlying reason for the interest in these structures. Therefore, we will describe the tuning of several different properties in some detail, thus highlighting the amount of property adjustment and control that is currently achievable.

3.1. Tuning of the size, shape, and spacing of arrayed nano-particles

For any technique to fabricate nanostructures, the ability to tune the structural parameters such as shape and size is important, since at the nanometer scale, many new phenomena and physical properties are closely related to the shape and size of the structures. Thus, the ability to adjust these parameters is a key to realizing nanostructures with novel properties. Anisotropic optical and magnetic properties have been found in metallic nano-rods [21,132], nano-particles [133,134], and nano-disks [135]. Another example is presented by the luminescence of semiconductor nano-rods that is strongly related to their shape [136]. Moreover, size is often a crucial nanostructure parameter. Some magnetic nanostructures show interesting properties as their size becomes comparable to the spin–flip diffusion length and magnetic domain-wall width [137]. For such reasons, good controllability of the shape and size of nanostructures has become one of the challenges in nano-technology and nano-fabrication.

For the UTAM nano-patterning approach, because the pore diameters of UTAMs can be controlled in the range of about 10–200 nm, the size of the surface nanostructures can be adjusted in the similar range. Moreover, using the pore-widening process, the pore diameter can be adjusted within the cell size of the pores. Thus, it is possible to control the spacing of the nano-particles at the same periodicity (equal to the cell size of the UTAM pores). So far, most nano-particles that were fabricated using UTAM nano-patterning are prepared using UTAMs anodized in 0.3 M oxalic acid solution at 40 V. The cell size of this UTAM is about 105 nm while the pore diameter is usually adjusted in the range of 50–80 nm, resulting in nano-particles with similar sizes. Recently, UTAMs prepared in sulfuric acid solutions with smaller cell size and pore diameters of about 65 and 45 nm were used and arrayed nano-particles with smaller pore size and period were successfully fabricated [48] (Fig. 15). The smallest nano-particles that were obtained in the process had a diameter as small as 20 nm (Fig. 15c).

In the UTAM fabrication of nano-particles using vapor-phase deposition processes, it is found that due to the closure effect of the pores of the top layer on UTAMs, the shape of the nano-particles changes with the evaporation process, which finally results in conical-shaped nano-particles (e.g. the nano-particles in Fig. 15c and Refs. [16,59]). Recently, a detailed investigation on the shape of nano-particles indicates that, by changing both the aspect ratio of the apertures of the UTAMs and the evaporation process (thickness of the deposited materials), the shape of the nano-particles can be adjusted, resulting in nanometer-sized disks, hemispheres, hemiellipsoids, and conics [48]. Fig. 16 shows a
A typical example of this shape tuning: a set of four samples was fabricated using four different UTAMs, which were prepared in oxalic acid solution under almost identical conditions except for different thicknesses of the UTAMs. The cell sizes of these UTAMs are about 105 nm and the pores were widened to about 80 nm. It is found that as the aspect ratios of the apertures of the UTAMs are different, which are about 1:3 (a), 1:4 (b), and 1:10 (c). The diameters of the nano-particles are about 45 (a), 40 (b), and 20–40 nm (c), respectively.
Fig. 17. AFM section analysis of the shape tuning of nano-particles. Samples in (a), (b), (c), and (d) are exactly the same samples in (a), (b), (c), and (d) in Fig. 16, respectively. The height and the base diameter of the discs (a), hemispheres (b), hemiellipsoids (c), and conics (d) are about 1.5 and 80 nm, 35–40 and 75 nm, 50–55 and 65 nm, 55–60 and 60 nm, respectively. To accurately reflect the particle shape, same dimension scale for the horizontal and vertical coordinates is used in the cross-sectional profile plot in (b), (c), and (d). Because the end of the AFM tip cannot be perfect sharp and there is a finite curvature even for high-aspect-ratio tips, the horizontal size (base diameter) of the nano-particles obtained from the AFM measurement is slightly larger than the actual size (about 4–5 nm larger).
ratio of the apertures of the UTAMs changes from about 1:2 (a), to 1:3 (b), 1:4 (c), and 1:8 (d), and the thickness of the deposited materials changes from about 1.5 (a), to 35–40 (b), 50–55 (c), and 60 nm (d), the shape of the nano-particles changes from disks (a), to hemispheres (b), hemiellipsoids (c), and finally to conics (d), i.e. the increasing of the pore aspect ratio and deposited materials thickness gradually sharpen the top of the nano-particles. In this shape changing process, the period of the nano-particles is kept constant at about 105 nm. A precise characterization of the shape of the nano-particles was carried
out using AFM section analyses with high-aspect-ratio AFM tips (Fig 17). The height and base diameter of the nano-particles are about 1.5 and 80 nm (a), 35–40 and 75 nm (b), 50–55 and 65 nm (c), 55–60 and 60 nm (d), respectively. The results clearly indicate that the shapes of the nano-particles are disk-like (a), hemispherical (b), hemiellipsoidic (c), and conical (d).

The observed shape tuning of the nano-particles arise from the pore closure effect in the evaporation process and the shadowing effect of the UTAMs (Fig. 18). At the beginning of the deposition, the top layer that formed on the UTAM has a similar pore size as that of the UTAM, which results in nano-particles with flat top surfaces, i.e. nano-disks. With the deposition progressing, there is a closure effect of the pores of the top layer which will lead to a continuous shrinkage of the pore size. This will sharpen the top of the nano-particles gradually, resulting in hemisphere and hemiellipsoid nano-particles. Further evaporation will clog the pores and lead to conical-shaped nano-particles. Therefore, due to the closure effect, a maximum height of the deposited nano-particles exists for a given evaporation condition. UTAM with smaller pores have an enhanced closure effect because the pores are easier to be blocked.

It is known that the channels of the UTAMs are unlikely to be perfectly smooth cylinders that are perpendicular to the substrate. Corrugations along the channels give rise to shadowing, especially when the aspect ratio of the channels is high. Moreover, it is usually impossible to achieve a perfect parallel between the evaporation direction and the channels of the UTAMs. These conditions lead to the shadowing effect of the pore walls of the UTAMs, which will lead to a residual attachment of the deposited materials on the pore walls. With increasing aspect ratio of the pores, the shadowing effect is enhanced and the diameter of the deposited nano-particles decreases. It is reported that when using 2 μm-thickness UTAM, the maximum height of the nano-particles is only about 10 nm [82]. However, using UTAMs with a similar pore size (i.e. similar closure effect due to the top layer) but much smaller thickness (<650 nm), the maximum height of the nano-particles is about 60 [43,45,48] or 80 nm [59]. This implies that the shadowing effect may also close the UTAM pores with the progress of the evaporation, and consequently also leads to a sharpening of the top of the nano-particles.

Fig. 18. Schematic outline of the closure effect and shadowing effect for the shape tuning. (a), (b), (c), and (d) correspond to the UTAMs and nano-particles in Fig. 16(a), (b), (c), and (d), which are nanometer-sized disks, hemispheres, hemiellipsoids, and conics, respectively.
The shape tuning in Figs. 16–18 originates from both the closure effect of the top layer and the shadowing effect of the pore walls. However, these two effects are parallel processes which can be used to adjust the particle shape separately. Using similar UTAMs with not only the same pore size but also the same pore aspect ratio (i.e. similar shadowing effect), a similar trend of shape tuning as that in Figs. 16–18 can be obtained just by changing the thickness of the deposited materials, i.e. the closure effect of the top layer in the evaporation process. On the other hand, by tuning the pore aspect ratio of UTAMs with the same pore size and same thickness of the deposited materials (i.e. same closure effect), the shadowing effect of the pore walls can be controlled and thus the shape of the nanoparticles can be adjusted.

The above explained shape tuning of nanoparticles are applicable to almost all vapor-phase deposition processes in fabricating surface nanoparticles, such as vacuum (thermal and E-beam) evaporation, sputtering, CVD, PLD, and MBE. However, it is found that [44] using MBE to deposit nanoparticles with an extremely slow deposition rate
(0.04 monolayer/s = 0.012 nm/s, monolayer thickness = 0.3 nm) will result in an irregular top layer composed of isolated islands on the UTAM instead of a regular and continuous top layer. This will lead to an irregular closure effect of the top layer and decreases the shape uniformity and adjustability of the nano-particles. It should be mentioned that such a slow deposition rate is seldom used for most vapor-based deposition processes. For example, the deposition rates used for synthesizing the nano-particles in Fig. 16 are in the range of 0.15–0.3 nm/s, which are already slow deposition rates for fabricating nano-particles.

Recently, Park et al. reported that using a high density plasma RIE etching process, it is possible to adjust the shape of NbO$_x$ nano-particle from pillars to conical-shape particles [70]. The NbO$_x$ nano-pillar arrays were fabricated by fully anodizing Al/Nb/Si [71]. Fig. 19 shows the shape change with the RIE etching process. The as-prepared NbO$_x$ nano-pillars had a mushroom-like shape. With high density plasma etching, the top part of the nano-pillar shrinks while the stem of the nano-pillar expands, resulting in cylindrical and finally conical nano-particles. This process provides an additional way to adjust the shape of the nano-particles that were fabricated using the UTAM technique.

3.2. Metal nano-particle arrays and the electronic, optical, and magnetic properties

Metal nano-particle arrays on substrates with high density and regularity are well-suited for the fabrication of magnetic recording media, optical sensors, and photonic devices. Using the UTAM nano-patterning approach, different metals have been fabricated into ordered nano-particle arrays on substrates. Some of them show interesting electronic, optical, and magnetic properties that are closely related to the adjustable structures and architectures of the ordered nano-particle arrays.

3.2.1. Electron transport properties

In recent years, research that focuses on single-electron behavior in molecular electronics devices has raised increased attention due to future possibilities for ultimate integration densities as well as due to new options for analyzing charge transport in the quantum regime. In this context, defined nanostructures on surfaces can be of importance in measuring the transport characteristics of nano-scale systems. One example is given by ordered Al nano-particle arrays on SiO$_2$/Si substrates fabricated by Shingubara et al., that show a non-linear current–voltage characteristic, which strongly suggests Coulomb blockade behavior due to a single electron charging effect [81]. The Al nano-particles were fabricated using a nano-indentation pretexturing process and a subsequent anodization (Fig. 20a–c). Instead of using a SiC mold for imprinting, the pretexturing process was accomplished using AFM indentation to create holes on an Al layer. The surface-patterned Al layer was anodized through the Al layer and the anodization stopped when the bottom of the barrier layer reached the surface of the Si. Afterwards, the aluminum oxide was removed, leaving Al nano-particle arrays on Si. Tetragonal and hexagonal arrays of Al nano-particles can be fabricated from the corresponding configuration of the initial indentation hole arrays. Current–voltage measurements were carried out using FIB-deposited W electrodes connecting a 23 × 15 Al particle array between the electrodes (Fig. 20d). Non-linear current–voltage characteristics were found for the Al nano-particles both at room temperature and at low temperature (4.2 K). There is an obvious step in the current–voltage curve near zero voltage with an offset of about 0.13 V (Fig. 20f). This current step originates from the Coulomb blockade due to single electron tunneling along a row of
Al nano-particles over the oxide barriers between the nano-particles. Although the field of electron transport through nano-scaled – or even molecular structures presents a field of current interest, it would be the matter of a different review to capture even the major research work. Thus, the topic of electron transport through nanostructures will not be followed within this review, but instead we will focus on structure/property relations of highly ordered nanostructures.

3.2.2. Tunable optical properties

Plasmon resonance based on nanometer-sized metallic particles is an important process in obtaining selective optical transmission and absorption spectra. It has potential applications in many fields, such as optical lithography, sensing devices, and Raman spectroscopy. Ordered metal nano-particle arrays on substrates are ideal candidate structures for the plasmon resonance because of the highly ordered and dense arrangements of the nano-particles. Recently, it was confirmed that [58,59] ordered Au nano-particle arrays on substrates have excellent plasmon resonance performance with high sensitivity to the surrounding liquid medium, with optical anisotropy, and with electric-field tuning behavior.

Matsumoto et al. studied the absorption spectra of ordered Au nano-particle arrays fabricated using the UTAM approach [59] in transmission geometry. It was found that the peak position ($\lambda_{\text{max}}$) of the transmission absorption spectra of the Au nano-particle arrays can be adjusted by changing either the height of the nano-particles ($h$) or the refractive index ($n$) of the surrounding media (liquid or gas). Fig. 21 shows the dependence of the peak position of the transmission absorption spectra on the refractive index of the surrounding medium. The peak position shows a red-shift to higher wavelengths with increasing refractive index (Fig. 21I). The shifts of the peak positions $\Delta\lambda_{\text{max}}$ have a linear
relationship with the refractive index (Fig. 21II). Moreover, the sensitivity factors of the dependence of the peak shift on the refractive index of the surrounding medium \( \frac{\Delta k_{\text{max}}}{\Delta n} \) and on the particle height \( \frac{\Delta k_{\text{max}}}{\Delta h} \) are apparently higher than those observed on disordered or low density nano-particle arrays. This is caused by the high density arrangements and high ordering of the Au nano-particle arrays fabricated using the UTAM nano-patterning. This indicates the prospect to fabricate optical sensors using UTAM-prepared ordered metal nano-particle arrays.

The plasmon resonance behavior of ordered Au nano-particle arrays was also investigated by Kossyrev et al. [58]. Au nano-particle arrays display a strong anisotropic absorption feature which is shown in Fig. 22a. The normal-to-substrate plasmon oscillations...
increase while the lateral-to-substrate plasmon oscillations decrease when the incident angle of the light changes from 0° to 40°. The reason for this optical anisotropy is attributed to a group of non-interacting individual particles in the normal direction and a collective ensemble within the nano-particle matrix in the lateral dimension. Interestingly, the absorption spectra of the Au nano-particle/liquid crystal matrix can be tuned by an electric field (Fig. 22b). A 2 V/μm applied electric field results in a blue shift of the peak position of the normal plasmon mode and a red shift of the lateral plasmon mode. This electric field-off and -on behavior of the absorption spectra of the ordered nano-particle arrays may be useful for the fabrication of photonic nano-devices with tunable colors.

3.2.3. Magnetic properties

Device miniaturization for obtaining ultra-high density data storage devices drives the development of nanometer-sized magnetic structures, such as dense nano-magnet arrays on substrates. Due to the high density and regularity, magnetic metal nano-particle arrays fabricated using the UTAM nano-patterning are desirable materials for ultra-high density magnetic recording systems.

An important issue accompanying the miniaturization is the thermal stability of the magnetic nanostructures. It is well-known that, as the nano-particles become smaller, the effects of thermal fluctuation become significant. Due to the small size, the magneto-crystalline anisotropy energy decreases and so does the temperature above which thermal fluctuations of the magnetization direction average out the residual magnetic field. This effect is called “superparamagnetism” and is undesirable in magnetic recording systems. An effective approach to overcome the problem is using the exchange anisotropy in ferromagnet/antiferromagnet systems to stabilize the magnetization. Liu et al. fabricated ordered nano-particle arrays of Fe on an antiferromagnetic FeF₂ layer [47] and on a MgO substrate. The magnetic hysteresis loops of the Fe/FeF₂ and Fe/MgO at 10 K are shown in Fig. 23. It is found that the remanent magnetization and the squareness of the
hysteresis loop of the Fe/FeF₂ structure (exchange biased) is obviously improved compared to those of the Fe/MgO (unbiased). This improvement mainly originates from the exchange anisotropy of the Fe/FeF₂ structure, which indicates that ferromagnetic/antiferromagnetic exchange bias can be used as an anisotropy source to stabilize the magnetization in the nano-particle arrays and hence to improve the magnetic performance.

3.3. Semiconductor nano-particle arrays and their properties

Semiconductor nano-particle arrays on substrates present the most important examples of surface nanostructures and have the largest relevance for current or near-term applications, such as electronic and photonic devices, sensors, solar cells, and memory devices. Ordered nano-particle arrays of many semiconductors, which include Si-based, Ge-based, III–V, II–VI, and oxide semiconductors, have been prepared on substrates using the UTAM nano-patterning approach. In this section, different types of semiconductor nano-particles will be introduced separately.

3.3.1. Si-based nano-particle arrays

Si has an indirect band structure where radiative recombination is strongly disfavored by a large mismatch between the electron and hole states and by a competition with non-radiative processes. This situation greatly limits the light emission from Si. Phonon localization is a good method to achieve light emission in Si, both in the case of phonon confinement in quantum-sized Si crystallites and for high concentrations of dopants or defect centers in Si. Recently, ordered arrays of Si and Er-doped Si nano-particles were fabricated using the UTAM patterning approach and phonon confinement and strong photoluminescence (PL) were obtained [56,65].

Cloutier et al. fabricated ordered Si nano-particle arrays on Si-on-insulator (SOI) substrates by a RIE etching process using UTAM-fabricated metal nano-particles as etching caps [65]. Raman measurements on the Si nano-particle arrays show a larger asymmetric broadening and a shift towards lower wavenumbers compared to original SOI and bulk Si (Fig. 24). Such large downshift and asymmetric broadening of the optical-phonon peak of Si originate from phonon confinement in the quantum-size range, i.e. at sizes smaller than approximately 10 nm. This result was confirmed by further Raman measurements indicating that the shift and broadening of the optical-phonon peaks are both dispersive and excitation-power dependent. It was suggested that the phonon-localization centers are given by ultra-small crystallites that were formed in the surface layer of the Si nano-particles during the RIE process. This phonon confinement could favor radiative recombination and light emission and hence modify the optical properties of indirect band-gap Si structures.

Ordered Er-doped Si (Si:Er) nano-particle arrays were fabricated by Park et al. using pulsed laser deposition (PLD) and a post-annealing process in air [55,56]. There are almost no changes in the size, shape, and spacing of the arrayed Si:Er nano-particles after the post-annealing process. PL measurements show a strong emission peaked at 1.54 μm for both the post-annealed and as-prepared Si:Er nano-particle arrays (Fig. 25). This PL emission at 1.54 μm originates from the energy transfer from Si to Er³⁺ and the subsequent transition from the excited (⁴I₁₃/₂) to the ground (⁴I₁₅/₂) state in Er³⁺ ions. Moreover, it is found that the post-annealing processing may reduce the number of defects that act as non-radiative decay centers for Er³⁺, thus the PL intensity increases with the
post-annealing temperature. The ordered Si:Er nano-particle array with strong PL at 1.54 µm is a suitable material for efficient infrared optoelectronics devices. Other Si-based particles, hydrogenated Si (Si:H) nano-particle arrays on Si substrates, were fabricated by Ding et al. using UTAM nano-patterning and plasma-enhanced chemical vapor deposition (PECVD) [66]. It was found that the nano-particles are composed of ultra-small crystallites of about 3–6 nm in diameter. The small size of these Si crystallites gives rise to

Fig. 24. Raman spectra of bulk undoped silicon (solid line), original unpatterned SOI (open circle), and the silicon nano-particle array on SOI (solid circle) (reproduced from [65] with permission, copyright 2005, American Institute of Physics). (a) Tilted SEM image of the silicon nano-particle array with the scale bar 100 nm. (b) Raman microscope image of a SOI sample with scale bar of 3 µm.

Fig. 25. PL spectra of (a) as-prepared Si:Er nano-particle arrays and (b) nano-particle arrays after being annealed at 400 °C. The inset shows the change of PL intensity of 1.54 µm peak with variation of the post-annealing temperature (reproduced from [56] with permission, copyright 2005, American Institute of Physics).
Coulomb blockade features in the low-temperature current–voltage measurements on heterojunction structures of the Si:H nano-particles on Si.

3.3.2. Ge-based nano-particle arrays

Recently, using ordered germanium (Ge) nano-particle arrays embedded in a SiO$_2$ matrix, a metal–insulator–semiconductor (MIS) structure was fabricated and used as a memory nano-device [51]. The ordered Ge nano-particle arrays were fabricated using the UTAM nano-patterning approach via E-beam evaporation. The MIS structure is composed of four sub-layers on the Si substrate (Fig. 26a): a 5 nm-thick rapid thermal oxide (RTO) layer beneath 3 nm-thick Ge nano-particles, a 50 nm-thick oxide capping layer, and an Al gate electrode on the top. The RTO and capping oxide layers act as the insulator layer. A rapid thermal annealing (RTA) process was carried out at 1000 °C (device A) and 700 °C (device B) in N$_2$ for 200 s. Capacitance versus voltage ($C$–$V$) measurements show a counter-clockwise hysteresis for both devices A and B with charge densities of about 9·10$^{11}$ and 3·10$^{11}$ C cm$^{-2}$ (Fig. 26b), respectively. The charge density is higher than the estimated value based on the density of the Ge nano-particles of about 1.2·10$^{10}$ cm$^{-2}$. Most probably, this behavior is caused by the fact that the Ge nano-particles broke up into smaller nano-clusters after the annealing process, which is similar to the case of the MIS memory device with a Ge layer [138]. The good performance of the MIS memory structure based on the Ge nano-particles should originate from the high density and regularity of the Ge nano-particle arrays.

3.3.3. II–VI semiconductor nano-particle arrays

II–VI semiconductors, such as CdS, CdSe, and ZnO, have beneficial optical and opto-electronic properties. Ordered arrays of II–VI semiconductor nano-particle arrays on Si are expected to have novel and interesting optical properties due to their nanometer sizes and high regularity. Recently, using the UTAM nano-patterning approach, ordered nano-particle arrays of CdS [50], CdSe [48], and ZnO [57] were fabricated and present interesting optical properties.

![Schematic diagram](image)

Fig. 26. Schematic diagram (a) and $C$–$V$ characteristics (b) of MIS structures after RTA at 1000 °C for 200 s (device A) and at 700 °C for 200 s (device B).
CdS is an important II–VI semiconductor with a band-gap energy in the visible region (2.5 eV) and a relatively simple fabrication process. It was found that CdS nano-particles present novel properties and they have been widely used in solar cells, optoelectronics, and microelectronics. For the device application of CdS nano-particles such as in electronic and optical areas, it is usually desirable to fabricate large areas of ordered arrays of CdS nano-particles on substrates. Recently, using UTAM nano-patterning, ordered CdS nano-particle arrays with tunable PL properties were prepared on Si substrates [50]. The CdS nano-particles are polycrystalline particles that are composed of ultra-small

Fig. 27. Microstructures (cross-sectional HRTEM) of (a) CdS disk nano-particles (sample A) and (b) hemiellipsoid nano-particles (sample B). (a1) and (b1) are CdS nano-particles on substrates. (a2) and (b2) are crystallite-size estimation of the polycrystalline CdS nano-particles in (a1) and (b1), respectively. (a3) is a low-magnification image of arrayed CdS nano-disks and the UTAM.
and closely packed nano-crystallites. These crystallites increase in size as the duration of the CdS evaporation increases. Fig. 27 shows the change from disk-like nano-particles (sample A) to hemiellipsoid nano-particles (sample B) when the thickness of the nano-particles increases from about 10 to 50 nm. In this process, the size of the ultra-small crystallites increases from about 5–14 nm (Fig. 27a2) to 20–40 nm (Fig. 27b2). PL measurements of the CdS nano-particle arrays show a strong emission spectrum with two sub-bands that are attributed to band-edge and surface-defect emissions (Fig. 28). The peak position and width of the band-edge emission are closely related to the size of the crystallites in the CdS nano-particles. When the size of the crystallites increases from the quantum size region of about 5–14 nm to larger sizes of about 20–40 nm, the PL peak of sub-band I redshifts for about 33 nm while the width of sub-band I decreases. Moreover, the peak position of sub-band II is also related to the size of the crystallites. These results indicate that by adjusting the evaporation duration (thickness of the nano-particles), and hence varying the size of the crystallites in the nano-particles, it is possible to tune the PL properties of the CdS nano-particles, including the peak position and the width of the PL bands.

Another example of nanometer-sized II–VI semiconductor nano-particles with improved optical properties is presented by ordered ZnO nano-particle arrays fabricated by Xu et al. [57]. Temperature-dependent PL spectra show two ultraviolet peaks that originate from free and bound exciton emission and one visible peak that originates from oxygen vacancies (Fig. 29). The intensity ratio between the ultra-violet peak and the visible peak is about 400, which is much higher than that of the ZnO films that show an intensity ratio of about 20–40. This behavior originates from the oxygen-full ZnO deposition process and the large surface-to-volume ratio of the ZnO nano-particles, which provide a sufficient interaction of the ZnO nano-particles with oxygen during the deposition process.

![Fig. 28. PL spectra of samples A (a) and B (b) and their two Gaussian fit subbands. The peak positions of the sub-bands I and II are located at about 473 and 575 nm in (a) and 506 and 563 nm in (b), respectively.](image-url)
3.3.4. III–V semiconductor quantum dot arrays

Semiconductor quantum dots (QDs), especially the III–V semiconductor QDs, have attracted much attention recently due to their important applications in electronic and photonic devices [139]. The semiconductor devices based on QDs usually exhibit superior properties compared with traditional quantum well (QW) semiconductor devices. So far most studies on QDs have concentrated on strained heterostructures grown by self-organized MBE growth, which usually yields QDs with random positions and a broad size distribution [140]. Moreover, the self-organized growth of QDs is only applicable to lattice-mismatched heterostructures such as InAs/GaAs and InAs/InP. Additionally, the lattice-matched III–V semiconductor heterostructures such as GaAs/AlGaAs can only be fabricated by lithographic methods [141] which involve high cost and low throughput. Therefore, the UTAM nano-patterning approach is a desirable process for fabricating ordered III–V semiconductor QD arrays on substrates with lattice-matched heterostructures.

Mei et al. did systematic work on this topic and successfully obtained ordered III–V semiconductor QD arrays using the UTAM nano-patterning combined with a multiple deposition process [43–45]. First, ordered arrays of InGaAs/GaAs QDs on GaAs substrates were fabricated [43]. The structure of the InGaAs/GaAs QDs is a 4 nm In$_{0.32}$Ga$_{0.68}$As layer sandwiched between a 5 nm GaAs buffer layer and a 10 nm GaAs cap layer. Low-temperature cathodoluminescence (CL) measurements of the InGaAs/GaAs QDs show a clear CL peak around 920 nm that originates from the InGaAs QDs confined by GaAs barriers. This observation confirms the formation of the InGaAs/GaAs QDs and indicates that the UTAM-assisted MBE process is suitable for the growth of heterostructured QD arrays. Mei et al. further fabricated ordered arrays of GaAs/AlGaAs QDs [45], which is a lattice-matched heterostructure with technological importance. Both single-well and double-well GaAs/AlGaAs QDs were prepared and their optical properties were studied. The structure of double-well GaAs/AlGaAs QDs is shown in Fig. 30a and b. Besides a cap GaAs layer on the top and a buffer GaAs layer at the bottom, the QD...
consists of two 4 nm GaAs well layers, each sandwiched between two 6 nm AlGaAs layers. For single-well QDs, only one GaAs well layer is sandwiched between two AlGaAs layers. Both the single-well and the double-well QD arrays show sharper and stronger PL emission compared to that of a reference quantum well structure (Fig. 30c). This behavior originates from the good crystal quality and the high regularity of the QDs. The proposed UTAM-assisted MBE process is a promising approach to fabricate large areas of ordered arrays of III–V semiconductor QDs with lattice-matched heterostructures, and to successfully overcome the limitation of the self-organized growth in fabricating only lattice-mismatched QD heterostructures.

Similar InGaAsN:Sb/GaAs QD arrays were also fabricated by Kouklin et al. [46]. Instead of the multiple deposition process in fabricating QDs as performed by Mei et al., they used the UTAM nano-patterning etching process on a MBE-grown InGaAsN:Sb/GaAs QW to fabricate InGaAsN:Sb/GaAs QD arrays (Fig. 31). Using this method, ordered arrays of QDs with high aspect ratio (pillars) can be obtained (Fig. 31c) because there is no height limitation of the deposited nano-particles. PL measurements of the InGaAsN:Sb/GaAs QD arrays show higher PL emission intensity compared to the as-grown InGaAsN:Sb/GaAs QWs, which is caused by a stronger (electronic) hole localization in the QDs than that in the QWs. These ordered arrays of InGaAsN:Sb/GaAs QDs with high aspect ratio and good PL performance might be used in the fabrication of well-defined and controllable three-dimensional optical nano-devices.

Fig. 30. (a) Cross-sectional SEM image of a typical double-well GaAs/AlGaAs QD; (b) schematic diagram of layered structure in each QD; (c) Low-T (4.2 K) PL spectra of a single-well and a double-well GaAs/AlGaAs QD array, and a reference single quantum well (QW) (reproduced from [45] with permission, copyright 2003, American Institute of Physics).
Besides the fabrication of ordered arrays of GaAs-related QDs, some other III–V semiconductor nano-particles, such as InN, were also fabricated using the UTAM nano-patterning approach [54].

### 3.3.5. Metal oxide nano-particle arrays

A continuous anodization process (without changing the anodization voltage in the entire anodization process) on an Al/metal/substrate structure will lead to a connected UTAM and will also yield metal oxide nano-particles on the substrate. The metal oxide nano-particles are anodized from the metal layer between the Al and the substrate after the anodization of the Al layer. Ordered metal oxide nano-particle arrays can be obtained on the substrate after the removal of the UTAM. So far, this process has been used in fabricating different metal oxide nano-particle arrays, which include TaOₓ [71–75], NbOₓ [70,71], TiO₂ [76–78], and WO₃ [123]. Using a similar process on Al/Si structures, ordered

---

**Fig. 31.** Schematic diagram of the UTAM-assisted MBE growth of InGaAsN:Sb/GaAs QD arrays (a and b). (a) InGaAsN:Sb/GaAs QWs; (b) InGaAsN:Sb/GaAs QDs. (c) is the SEM image of an ordered array of InGaAsN:Sb/GaAs QDs with a pillar-like formation, the length and diameter of the nano-pillars are about 250 and 50 nm, respectively (reproduced from [46] with permission, copyright 2003, IOP Publishing Ltd.).

**Fig. 32.** Shape difference between (a) Ta₂O₅ pillar-like nano-particles (reproduced from [67] with permission, copyright 2004, The Japan Society of Applied Physics) and (b) NbOₓ mushroom-like nano-particles (reproduced from [70] with permission, copyright 2005, The Electrochemical Society, Inc.).
SiO$_2$ nano-particle arrays can also be fabricated via the anodization of the Si substrates after the Al anodization [79,108,109].

It is found that the shapes of the anodized TaO$_x$ (Ta$_2$O$_5$) and NbO$_x$ nano-particles are quite different (Fig. 32). The Ta$_2$O$_5$ nano-particles are pillar-like particles with a round top surface while the NbO$_x$ nano-particles are mushroom-like particles with a long stem. Mozalev et al. [71] demonstrated that this shape difference originates from the different anodization processes of Al/Ta/Si and Al/Nb/Si structures.

In the final anodization process of Al/Ta/Si (I–III in Fig. 33), after the bottom of the barrier layer touches the Ta surface, Ta$_2$O$_5$ forms between the alumina barrier layer and the substrate due to the cross-migration of the O$^{2-}$ and Ta$^{5+}$ ions. During the anodization, the alumina barrier layer dissolved at both the Al$_2$O$_3$/Ta$_2$O$_5$ and electrolyte/Al$_2$O$_3$ interface, and the Al pyramids between the cells keep on being converted into alumina. These two effects will finally cause the formation of arched barrier layer structures. This process is similar to the final anodization process of Al on a substrate without a metal layer.

![Fig. 33. Schematic diagram of the formation of the pillar-like Ta$_2$O$_5$ nano-particles (I–II–III) and the mushroom-like NbO$_x$ nano-particles (IV–V) (reproduced from [71] with permission, copyright 2003, Elsevier).](image)
(Section 2.3.3.1), except that instead of a void beneath the barrier layer, a Ta$_2$O$_5$ nano-particle formed between the arched barrier layer and the substrate. The top surface of the nano-particle is actually the bottom surface of the arched barrier layer, thus pillar-like nano-particles with round top surfaces are formed. It should be mentioned that the arched barrier layer will finally dissolve with further anodization. The nano-particle that formed before the disappearance of the barrier layer consisted of pure Ta$_2$O$_5$ while later a mixed aluminum–tantalum oxide layer forms in the top part of the nano-particle.

In the case of Al/Nb/Si (IV–V in Fig. 33), the oxidation process of niobium is much faster than that of the adjacent aluminum because the formed niobium oxide (Nb$_2$O$_5$) has a lower ionic resistivity than that of alumina. This causes a narrow and perpendicular channel beneath the bottom of the barrier layer. The cross-migration of Nb$^{5+}$ and O$^{2-}$ ions in the oxidation of niobium and the concurrent barrier layer dissolution only take place along this narrow channel, and finally result in the stems of the mushroom-shaped nano-particles. With further anodization the Nb$_2$O$_5$ grows beyond the pore bottom and the outer part of the alumina oxide cell will take part in the anodization process of the niobium, forming the top of the mushroom. It should be mentioned that only the stem part of the mushroom is pure Nb$_2$O$_5$ while the top is mixed niobium–aluminum oxide.

It is found that TiO$_2$ [76–78] and SiO$_2$ nano-particles [79] that are fabricated using this method have the similar shape as that of the Ta$_2$O$_5$ particles, indicating the occurrence of similar anodization processes as in the case of Ta$_2$O$_5$. However, the mushroom-shaped nano-particles are so far limited to Nb$_2$O$_5$. It would be interesting to apply the anodization process to other metals to explore possible new shapes of the anodized nano-particles.

The anodization process for fabricating metal oxide nano-particles is a continuous process without changing the anodization voltage. As introduced in Section 2.3.3, the anodized metal oxide layers such as TiO$_2$, can be removed or penetrated using a ramped or reversed voltage, or simply a pore-widening process.

![Fig. 34. Fabrication process of the nano-scale two-electrode field emission arrays (reproduced from [77] with permission, copyright 1999, American Vacuum Society): (1) substrate; (2) Ti; (3) Al; (4) cell; (5) pore; (6) wall; (7) barrier layer; (8) TiO$_2$; (9) Ti; (10) Ta; (11) Al; (12) tip; (13) Al; (14) Ta$_2$O$_5$.](image-url)
Using ordered TiO₂ nano-particle arrays, a nano-scale field emission array was fabricated by Tatarenko et al. [77]. The field emission array was prepared by first anodizing a binary Al/Ti layer on a substrate, resulting in an UTAM and TiO₂ nano-particles (Fig. 34). As the next step, the UTAM/nano-particle/substrate structure was covered with top Ta and Al layers, forming a two-electrode nanostructured emission device with a 150 nm distance between the electrodes. The obtained particle packing density in these structures was about $4 \times 10^{10} \text{cm}^{-2}$. The field emission measurement of the nano-particle arrays performed both in vacuum with an electrode distance of 300 µm and in air in the two-electrode emission device, confirmed the field-emission characteristics of these structures described by the Fowler–Nordheim law. The effective field emission voltage was 2.7 V for the two-electrode emission device, which is considerably less than the value of the first-ionizing-potential of air at atmospheric pressure. When the electron free path length in air is longer than the distance between the anode and the cathode in the two-electrode emission structure, the field emission devices can operate perfectly in air.

4. Highly ordered nano-hole arrays

In the past, several techniques have been reported to be capable of creating ordered nano-hole arrays on the surfaces of substrates. One example is obviously given by the anodization of Al itself. Recently, using the UTAM nano-patterning approach, ordered nano-hole arrays were fabricated on semiconductor, diamond, and metal substrates [60–64,83–107]. Due to the distinct advantages of the resulting nano-hole arrays such as high pore regularity and high area density, this surface nanostructure has demonstrated novel and interesting properties that can be used in the fabrication of antireflection materials, high density electronic devices such as capacitors and electrodes, photonic crystals and waveguides, and device-level optical or lasing materials. This section reviews the current state of the art in this field.

4.1. Features in the etching process

To etch holes on substrates through the pores of the UTAMs, the dry etching processes that were used for the UTAM nano-patterning approach should have anisotropic character. So far there are four dry etching processes that have been used for hole etching on substrates: reactive ion etching (RIE), plasma etching (PE), fast atom beam (FAB) etching, and ion milling. Table 3 lists the details of the etching conditions concerning the different etching processes. The substrates include many semiconductors such as Si, GaAs, GaN, InP, ZnTe, and other materials such as diamond and Al.

It is found that when the thickness of the UTAMs is about 1.0–1.5 µm, holes are absent in a number of small areas on the substrates [61], or even no holes are formed on the substrates [84]. This indicates that there is a shadowing effect of the pore walls of the UTAMs to the etching, which is quite similar to the evaporation process in fabricating nano-particles on substrates using UTAMs. A smaller thickness of the UTAM will decrease the shadowing effect and hence facilitate the hole etching. However, the thickness of the UTAMs should not be too small because the UTAMs are also etched in the etching process. Normally, the thickness of the UTAMs for the hole etching process is in the range of 300–700 nm.
<table>
<thead>
<tr>
<th>Ref. no.</th>
<th>Nano-holes on substrates</th>
<th>Etching method</th>
<th>Gas</th>
<th>Flow rate (sccm)</th>
<th>Pressure (mTorr)</th>
<th>Power (W) or V/I</th>
<th>Etching rate, nm/min and (mask thickness, nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[60]</td>
<td>Si</td>
<td>IM</td>
<td>Ar</td>
<td></td>
<td></td>
<td></td>
<td>Low</td>
</tr>
<tr>
<td>[61]</td>
<td>GaAs</td>
<td>RIE</td>
<td>BCl3/Cl2/SiCl4</td>
<td>25:1:5</td>
<td>5</td>
<td>100</td>
<td>~6</td>
</tr>
<tr>
<td>[63]</td>
<td>Si</td>
<td>PE</td>
<td>BCl3</td>
<td>20</td>
<td>15</td>
<td>100</td>
<td>6 (500)</td>
</tr>
<tr>
<td>[63]</td>
<td>GaAs</td>
<td>RIE</td>
<td>Cl2</td>
<td>60</td>
<td>80</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>[84]</td>
<td>GaAs</td>
<td>RIE</td>
<td>Br2/N2</td>
<td>0.11:0.54</td>
<td>40</td>
<td></td>
<td>~8 (500)</td>
</tr>
<tr>
<td>[85]</td>
<td>InP</td>
<td>RIE</td>
<td>BCl3/Cl3</td>
<td>2.70</td>
<td>50</td>
<td>450 V</td>
<td>150</td>
</tr>
<tr>
<td>[90]</td>
<td>Si</td>
<td>FAB</td>
<td>SF6</td>
<td>6.7</td>
<td></td>
<td>2 kV/35 mA</td>
<td>23.3 (700)</td>
</tr>
<tr>
<td>[91]</td>
<td>Si</td>
<td>PE</td>
<td>Cl2/Ar</td>
<td>15:5</td>
<td>8</td>
<td>200</td>
<td>200 (500)</td>
</tr>
<tr>
<td>[92–95]</td>
<td>Diamond</td>
<td>PE</td>
<td>O2</td>
<td>150 (20 Pa)</td>
<td>150</td>
<td></td>
<td>16.7</td>
</tr>
<tr>
<td>[96]</td>
<td>Diamond</td>
<td>FAB</td>
<td>O2</td>
<td>20</td>
<td></td>
<td>3 kV</td>
<td>4.2</td>
</tr>
<tr>
<td>[97]</td>
<td>GaAs</td>
<td>FAB</td>
<td>Cl2</td>
<td></td>
<td>0.00048</td>
<td>1 kV</td>
<td>66.7</td>
</tr>
<tr>
<td>[100,101]</td>
<td>GaN</td>
<td>PE</td>
<td>CF4/He</td>
<td>20:20</td>
<td>10</td>
<td>500</td>
<td>2.75 (400)</td>
</tr>
<tr>
<td>[105]</td>
<td>Al</td>
<td>PE</td>
<td>Cl2/Ar</td>
<td>20:5</td>
<td>8</td>
<td>200</td>
<td>~2000 (600)</td>
</tr>
</tbody>
</table>

Abbreviation in the table: IM = ion milling; RIE = reactive ion etching; PE = plasma etching; FAB = fast atom beam.
A precondition of the UTAM etching for fabricating nano-holes (especially deep holes) on substrates is that the etching rate of the UTAM should be much smaller than that of the substrate. Actually this is the case in the above-mentioned etching processes for the UTAM hole etching. Nakao et al. gave a detailed analysis [84] of the etching rates of the UTAM, of the UTAM-covered GaAs and of the bare GaAs substrate (Fig. 35). It is clearly shown that after 100 min etching, the etching depth in the bare substrate area is about 10 times deeper than the hole depth in the UTAM-covered area (Fig. 35a). Additionally, the etching on the UTAM is very small. The results are plotted in Fig. 35b. After 100 min RIB etching, the etching depth on the UTAM is less than 0.2 \mu m, while the etching depth of the UTAM-covered GaAs area and the bare GaAs area is about 1 and 10 \mu m, respectively. This means that the UTAM selectivity (ratio of the etching rates) is more than 50 for bare GaAs and more than 5 for UTAM-covered GaAs.

The UTAM-assisted etched holes usually have a slightly conical cylindrical shape (Fig. 36a). In extreme cases, it could be a quasi-conical shape (Fig. 36b). This shape is caused by the lateral etching on the hole walls. Although the etching is an anisotropic etching mainly in the direction along the long axis of the holes, there exists a weak lateral etching perpendicular to the hole wall. This etching will gradually etch the walls and widen the holes, finally resulting in slightly conical cylindrical holes. Although this lateral etching is weak, a very long etching process could remove most of the hole walls in the top layer of the etched holes, resulting in a surface-tapered pattern, which is shown in Fig. 36c. In this surface-tapered pattern structure, cylindrical holes still exist in the bottom layer of the etched holes while in the top layer, the Si surface is tapered periodically. Another possible reason for the slightly conical holes is that the substrate material that is etched from the holes attach on the pore walls of the UTAM. This effect will increase the shadowing effect of the UTAMs and gradually decrease the hole size.

The etching rate of the holes is dependent on many factors including (please refer to Table 3) UTAMs, etching conditions and substrates:
UTAMs. It has been mentioned that the etching rate of holes decrease to zero when the thickness of the UTAM is beyond some limitations such as 1.5 μm [84]. Moreover, the pore size of the UTAMs also influences the etching rate. It is found that, with similar etching conditions and UTAM thickness, the etching depth of the GaAs holes using a 60-nm-

Fig. 36. Shape of the nano-holes: (a) slightly conical cylindrical shape (reproduced from [84] with permission, copyright 1999, The Japan Society of Applied Physics); (b) quasi-conical shape (reproduced from [61] with permission, copyright 2002, Wiley-VCH Verlag GmbH); (c) surface-tapered shape (reproduced from [90] with permission, copyright 2001, American Institute of Physics).
diameter UTAM is about 10% shallower than that of using a 80-nm-diameter UTAM [84]. This implies that the actual factor that influences the etching rate is the aspect ratio of the UTAM pores rather than the thickness of the UTAM.

**Etching conditions.** The etching conditions, including the etching process, gas and its flow rate and pressure, and the power of the etching, can greatly change the etching rate. For example [105], for a low RIB etching power of 100 W, holes cannot be obtained on Al foils. When the power is higher as 300 W, the pore structures of the UTAM were destroyed very fast and thus ceased the hole etching on substrates. Two hundred Watts is approved to be a suitable power for the hole etching on Al foil.

**Substrates.** The etching rate of holes is also largely dependent on the specific substrates. For example, using similar plasma etching conditions (see Refs. [91,105] in Table 3), the etching rate on Al foils is about 10 times higher than that on Si substrates, suggesting a much easier etching of Al compared to Si.

### 4.2. Si nano-hole arrays with antireflection properties

For antireflection structures such as surface hole (or grating) arrays, the antireflection properties are improved by increasing the hole depth and decreasing the hole period [142]. Thus, highly ordered nano-hole arrays on substrates yield desirable antireflection structures because the nanometer-sized deep holes can greatly suppress the reflection over a wide spectral bandwidth. Recently, ordered Si nano-hole arrays fabricated using the UTAM nano-patterning have been shown to present excellent antireflection behavior [90,91].

Kanamori et al. [90] found that an overetched Si surface with surface-tapered nano-hole pattern (Fig. 36c) functioned as a fine two-dimensional antireflection structure. As shown in Fig. 37a, the reflectivity of the Si nano-hole structure is less than 1.6%, which is tremendously smaller than the reflectivity of the Si substrate of about 40%. This antireflection mechanism of the Si nano-hole structure is applicable to a wide range of wavelengths from 400 to 800 nm.
400 to 800 nm. A similar experiment of Tian et al. [91] confirmed this point and additionally found that the Si nano-hole arrays have an obviously lower reflectance compared to that of the bulk Si substrate (Fig. 37b). The antireflection of the nano-holes improves with increasing hole depth and also covers a wide wavelength range from about 207 nm (6 eV) to 620 nm (2 eV). Tian et al. also investigated the effect of the antireflection surface on the scattering behavior. It is found that the nano-holes on the surface enhanced both insertion and extraction efficiencies. The antireflection performance of the Si nano-hole structure in a wide wavelength range is very attractive concerning the application of optical devices.

4.3. GaAs nano-hole arrays: a photonic crystal used as waveguide

Photonic crystals have periodic structures with periodicities of the order of the wavelength of the light. Usually the periodic structures of the photonic crystals are fabricated using conventional lithographic approaches. Using the UTAM nano-patterning, Nakao et al. demonstrated the fabrication of photonic crystal structures of ordered GaAs nano-hole arrays [97]. The UTAMs were fabricated using a pretexturing process, which results in UTAM pores and etched GaAs holes with large defect-free areas. The light scattering measurements were carried out using a YAG laser to illuminate the GaAs nano-hole samples (Fig. 38). The light scattering from the nano-hole part (position a) shows a marked polarization sensitivity, which is a typical feature of photonic crystals. Moreover, the scattering intensity of the H-polarization (perpendicular to the hole axis) light from the nano-hole part (position a) is more than twice as large as that from the substrate part (position b), which further confirms the photonic crystal nature of the GaAs nano-hole arrays. A photonic band-gap waveguide was obtained based on these ordered GaAs nano-hole arrays (Fig. 39). A bending line consisting of a defect of the photonic crystal periodicity was fabricated on the GaAs nano-hole arrays and acted as the light waveguide (inset in Fig. 39). From the infrared CCD image, it was observed that the light was

![Fig. 38. Infrared CCD image of the GaAs nano-hole arrays (reproduced from [97] with permission, copyright 2002, Springer Science and Business Media). The YAG spot laser illuminates positions a (A) and b (B). a is on the GaAs nano-hole part while b is on the underlying GaAs substrate part (C).](image-url)
scattered along the bending line, forming a photonic band-gap waveguide. These experiments confirm that the highly ordered nano-hole arrays fabricated using the UTAM nano-patterning are excellent structures for photonic crystals and waveguides.

4.4. Ordered nano-hole arrays in fabricating high quality device-level GaN layers

GaN-related semiconductors have been intensively studied in the last decade due to their applications in optoelectronic devices such as light emitting and laser diodes with green, blue, and violet emissions [143]. Nanometer-sized GaN structures such as nano-particles, nano-holes, and nano-wires, especially with the configuration of highly ordered nanostructure arrays, are expected to have improved optoelectronic properties.

Liang et al. first attempted to use the UTAM nano-patterning approach to fabricate GaN nanostructures [83]. Ordered nano-hole arrays were dry-etched on Si(1 1 1) substrates using the UTAM nano-patterning. GaN films were then epitaxially grown on this nano-patterned Si surface. Room temperature PL measurements indicated that the intensity of the GaN films grown on nano-patterned Si is five times higher than that of the GaN grown on non-patterned Si (Fig. 40). Moreover, there is a 10 meV shift of the PL peak position. These results point to the high quality of the GaN film grown on nano-patterned Si with possible strain-relaxed GaN.

Wang et al. performed a systematic study on fabricating ordered GaN nanostructures based on the UTAM nano-patterning [100–103]. They first fabricated porous GaN films with ordered nano-hole arrays (Fig. 41a) by UTAM-assisted plasma etching [100]. Moreover, ordered GaN nano-pillar arrays (Fig. 41b) were obtained by further etching the
The formation of the nano-pillars is caused by overetching that leads to the partial removal of the pore walls of the etched holes, which is similar to the overetched tapered surface in Fig. 36c. The micro-PL of the GaN nano-hole arrays is similar to that of the as-grown GaN film (Fig. 41a'), which indicates the good quality of the nano-porous GaN film. Moreover, based on the PL and the micro-Raman measurements, the plasma etching process does not produce many defects on the surface of the GaN nano-porous films. The PL measurement on the overetched GaN nano-pillar arrays gave similar results (Fig. 41b'). The PL intensity of the nano-pillars is even higher than that of the as-grown GaN. Moreover, the low-temperature PL measurement shows a very weak impurity-related donor–acceptor pair (DAP) emission, which suggests a very low density of the etching-related defects on the GaN surface and further confirms the high crystallinity of the GaN nano-pillars.

As known, GaN films for device applications are mainly grown on substrates including sapphire, SiC, and Si. Due to the lattice and thermal mismatching, the heteroepitaxial growth of GaN typically involves high defect densities and residual strain inside the GaN film, which greatly degrades the performance of the GaN optoelectronic devices. Lateral epitaxial overgrowth (LEO) of GaN has been shown as an efficient growth technique to decrease the defect density in GaN films and hence to improve the device performance and reliability [144,145]. It was found that nanometer-sized porous materials, such as anodized porous SiC [144] and GaN [145], can be good overgrowth templates in the LEO process to avoid the creation of defects in GaN. However, most overgrowth templates so far are disordered porous structures with low structural controllability.

The ordered nano-hole arrays fabricated by UTAM nano-patterning present good overgrowth templates for fabricating GaN films with high quality. The above-mentioned work by Liang et al. is an attempt to use ordered Si nano-hole arrays as overgrowth template to fabricate GaN films [83]. However, because the GaN film was grown from Si nano-holes, the quality improvement of the GaN layer is limited. Recently, Wang et al. used UTAM-fabricated GaN nano-hole arrays [100] as LEO template and successfully fabricated high-quality GaN films.
quality GaN films with much lower defect density and internal strain [102]. They first fabricated ordered nano-hole arrays on a GaN layer using the UTAM method. Then a LEO GaN film was grown on the GaN nano-holes (Fig. 42a). It is clearly observed that the LEO GaN is grown from the small surface area between the holes, and there is no obvious GaN growth in the holes. Air-bridges (nano-holes) formed after the overgrown GaN coalesce at the top of the holes. From the top surface, it is found that the defect density in the LEO GaN film is much lower than that in the as-grown GaN (Fig. 42b and c). The high quality of the LEO GaN films was further confirmed by PL and Raman measurements.

Zang and Wang et al. further confirmed that ordered SiO$_2$ nano-hole arrays are also good LEO templates [103]. The SiO$_2$ nano-hole arrays were fabricated on a GaN film using the UTAM nano-patterning (Fig. 43I). The GaN film was then laterally overgrown on the SiO$_2$ nano-hole arrays. Truncated GaN pyramids were formed on the SiO$_2$ mask and finally coalesced, forming a continuous GaN LEO layer. Fig. 43II shows a truncated GaN pyramid grown on the SiO$_2$ template. It can be clearly seen that the SiO$_2$ template first “filtered” most of the defects in the GaN layer below the SiO$_2$ template. Due to the fast lateral growth and subsequent coalescence of the overgrown GaN from the SiO$_2$ template, vertical dislocations that passed through the SiO$_2$ template were forced...
to bend and finally most of these dislocations interacted with each other and disappeared within the first 50 nm region of the GaN overgrowth layer. Finally an almost defect-free GaN layer was formed.

All these results indicate that the ordered nano-hole arrays fabricated using the UTAM nano-patterning are suitable LEO templates for fabricating device-level GaN layers.

4.5. Diamond nano-porous films used as electrodes, capacitors, and imprinting molds

Diamond-related materials have been used in many fields due to their unique advantages such as high mechanical and chemical stability, high refractive index, and high thermal
conductivity. For example, porous diamond films can be used for filtration, heat-exchanging devices, and electrodes. Recently, nanometer-sized porous diamond films were fabricated by plasma etching using the UTAM nano-patterning [92–96]. These diamond nano-porous membranes have been used as electrical double-layer electrodes and nano-imprinting molds.

Masuda et al. fabricated two kinds of boron-doped diamond nano-porous membranes [92,95]: single-surfaced diamond films with nano-holes at only one side (Fig. 44a) and double-surfaced (through-hole) diamond films with nano-holes at both sides (Fig. 44b). Honda et al. studied the electrochemical properties of these diamond nano-porous membranes.
electrodes as electrical double-layer capacitors [93,94]. It is found that the nano-porous diamond films have wide electrochemical potential windows around 2.5 V, which is somewhat lower than that of unetched diamond films. The capacitance of the porous diamond film increases with increasing surface roughness. Diamond films with a hole diameter of 400 nm and a hole depth of 3 μm exhibited a 400-fold capacitance increase compared to the as-deposited diamond films. These nano-porous diamond films are suitable materials for the future development of capacitors and electrodes.

Usually the molds for the nano-imprinting process are patterned using the EBL method. Ono et al. demonstrated that ordered diamond nano-hole arrays that were fabricated using the UTAM approach can be used as nano-imprinting molds [96]. Large areas of PMMA nano-particle arrays on Si substrates were patterned using a nano-porous diamond film as the nano-imprinting mold (Fig. 45). Due to the low thermal-expansion and high hardness of the diamond, this nano-porous diamond mold is an excellent imprinting mold in fabricating large-scale ordered surface nanostructures.

4.6. Ordered arrays of electrolyte–molecule–silicon nano-capacitors

Molecule-based structures are potential materials for future nano-electronics devices. Recently, Zhao et al. reported the fabrication of ordered arrays of electrolyte–molecule–silicon nano-capacitors with interesting electrical properties [104]. Fig. 46 shows the structure of this nano-scale capacitor arrays. First an UTAM was fabricated on a LTO/SiN/a/Si substrate (LTO refers to low temperature SiO2). Subsequently, highly ordered nano-hole arrays were fabricated using RIE etching and a selective wet etching, until the surface of the Si was exposed. Finally, redox-active molecules (ferrocene) were attached to the exposed Si surface with O–Si bonds, resulting in ordered arrays of molecule/hole nano-structures. When the samples are immersed into electrolytes to measure the electrochemical properties, ordered arrays of nano-meter-sized electrolyte–molecule–silicon capacitors formed. Capacitance and conductance measurements of the nano-capacitor arrays show very high capacitance and conductance peaks near −0.6 V. The peaks are thought to originate from the charging and discharging of the electrons in the redox-active molecules. These results indicate the presence of reversible charge trapping which is important for possible memory nano-devices.

![Fig. 45. Diamond mold with ordered nano-hole arrays (a) and imprinted PMMA nano-particle arrays on a Si substrate (b) (reproduced from [96] with permission, copyright 2003, The Japan Society of Applied Physics).](image-url)
5. Other ordered nanostructures fabricated using the UTAM nano-patterning

Using the UTAM nano-patterning approach, other surface nanostructures can be fabricated besides the nano-particle and nano-hole arrays. These surface nanostructures include core–shell nano-particles that are oxidized from initial metal nano-particles, one-dimensional nanostructures (nano-wires and nano-tubes) fabricated from the catalyst nano-particle arrays on substrates, nano-rings or nano-dots fabricated using some special UTAM fabricating processes, and one-dimensional nano-materials fabricated in the pores of the UTAMs using electrochemical deposition. These special UTAM-related fabricating processes offer the prospect of a large potential for creating advanced structures and architectures, and also for synthesizing multifunctional materials with controlled and adjustable properties and property combinations. Thus, this chapter gives an overview of some structures and structuring techniques that are considered as especially promising.

5.1. Core–shell nano-particles with tunable nanostructures and optical properties

Core–shell nano-particles have been the subject of extensive research because such composite nano-particles have exhibited improved physical and chemical properties over their single-component counterparts, thus providing a new way to tailor the properties of the nano-particles. So far most of the approaches in fabricating core–shell nano-particles are based on wet-chemical methods. It is usually difficult to achieve highly ordered core–shell nano-particle arrays on substrates from such a wet-chemical method. Recently, it was demonstrated that, using a three-step oxidation process to oxidize ordered Indium nano-particle arrays prepared using the UTAM nano-patterning, ordered indium oxide coated indium core–shell nano-particle arrays can be fabricated with tunable optical properties [49].

The key to realize the core–shell nano-particles is a precisely controlled three-step oxidation process (Fig. 47). The first step is the preheating process. The temperature was held
at 146 °C for 1 h. One hundred and forty six degree celsius is around the melting point of the In nano-particles (about 10 °C lower than melting point 156.61 °C of bulk In). In the second step, the temperature was ramped to 800 °C at a rate of 10 °C min\(^{-1}\). The third step is the final oxidation process, in which the temperature was held at 800 °C for 2 h. A set of eight similar samples were analyzed to study the structural changes of the nano-particles in the 3-step oxidation process. The only difference of the eight samples is the oxidation duration. The time stop-positions of the eight samples (denoted as samples A–H) are marked in Fig. 47. Sample A are the initial In nano-particle sample. Samples C, E and H are the nano-particles after the preheating process, the temperature ramp process and the final oxidation process respectively. From the HRTEM and XRD measurement, it is found that In nano-particles (Fig. 48a) changed to In/In\(_2\)O\(_3\) core–shell nano-particles (Fig. 48b) and finally to In\(_2\)O\(_3\) nano-particles (Fig. 48c) [13]. This transition is schematically outlined in Fig. 49. At the beginning of the oxidation, a very thin oxide shell formed on the surface of the In particle (a). In the preheating process (a–c), the partially melted inner In core is oxidized at the core–shell interface by the diffused oxygen from the outer surface of the shell. Because the temperature is just around the melting point, the growth rate of the oxide shell is very small, about 5–6 nm/h. This slowly formed shell is extremely crucial to the formation of a stable In/In\(_2\)O\(_3\) core–shell particle from an In particle. For a normal oxidation process with a fast temperature increment, it is usually impossible to form a stable shell at the surface since the melted In will ‘bump into’ and break any new-formed oxide shell. In the three-step oxidation process, after the preheating process, a relatively thick and stable oxide shell (about 5–6 nm thick, see Figs. 48b and 49c) has been formed before the sample undergoes subsequent processing steps at higher temperatures. This is the reason why this 3-step oxidation process can realize the transformation of In particles to In/In\(_2\)O\(_3\) core–shell particles. In the following two processes, the inner In core is further oxidized at the core–shell interface with a higher transformation rate of about 10–11 nm/h. During the temperature ramp process (c–e), the shell thickness increases from about 5–6 nm to 16 nm. In the final oxidation process (e–h), the In core disappears, resulting in In\(_2\)O\(_3\) nano-particles. It is found that the final In\(_2\)O\(_3\) nano-particles are highly oriented single-crystal particles that originate from the single-crystal nature of the initial In nano-particles and the slow oxidation process [52]. The transformation
process from In nano-particles to In/In$_2$O$_3$ core–shell nano-particle and finally to In$_2$O$_3$ nano-particle. It is found that the PL of the core–shell nano-particles is closely related to their nano-structure and the oxidation process [49]. The peak position and intensity of the band-gap emission are determined by the oxide shell thickness while the intensity of the defect (oxygen vacancy) emission is changed with the oxidation process (the relation between the oxidation process and the density of the oxygen vacancies is also shown in Fig. 49). Therefore, by changing the shell thickness and the oxidation process, the intensity and peak positions of the PL from the core–shell nano-particles can be adjusted. This three-step oxidation process provides an attractive fabrication approach in fabricating ordered arrays of metal/oxide core–shell nano-particles with tunable optical properties.
5.2. Ordered arrays of one-dimensional nanostructures (nano-wires and nano-tubes) fabricated using ordered metal nano-particle arrays as catalyst

Ordered arrays of one-dimensional nano-materials, such as nano-wires and nano-tubes, have been intensively investigated due to their potential applications in many fields. In the catalytic growth of one-dimensional nano-materials, such as CVD and vapor–liquid–solid (VLS) growth, a key element in achieving uniform ordered arrays of nano-wires and nano-tubes is the control of the regularity and size of the catalyst particles. The template method, usually using the pores of anodic alumina membranes to confine the nano-wires or nano-tubes, forms an efficient approach in fabricating ordered arrays of one-dimensional nano-materials over large pattern areas with high throughput [20–37]. However, because most nano-wires and nano-tubes were fabricated in alumina membranes with a barrier layer and an aluminum layer at the backside, it is usually difficult to fabricate nano-wire or nano-tube arrays directly on substrates (such as Si), thus limiting their applications in Si-based microelectronics. Another disadvantage is that, because the pore walls of the membranes usually affect the catalytic growth of nano-wires and nano-tubes, the crystallinity of the nano-wires and nano-tubes fabricated in the pores of the alumina membranes are sometimes not high. For example, carbon nano-tubes (CNTs) prepared in the pores of alumina membranes usually have poor graphitization. This will also limit the properties and applications of the fabricated one-dimensional materials.

Using a mixed fabrication process of the UTAM nano-patterning and the catalytic growth of one-dimensional nano-materials, ordered arrays of nano-wire or nano-tube arrays can be fabricated on substrates with good crystallinity. First, ordered arrays of metal nano-particles (that will be used as catalysts in the following growth of one-dimensional nano-materials) are fabricated on the surface of substrates using the UTAM nano-patterning approach (Fig. 50a and b). The mask is subsequently removed and the growth of nano-tubes or nano-wires is carried out by catalytic growth processes (Fig. 50c and d). Because there is no alumina pore wall to affect the catalytic growth of the one-dimensional nano-materials, the crystalline quality of the nano-wires (or nano-tubes) should be better than that of the nano-wires (or nano-tubes) grown in the pores of the alumina membranes.
So far ordered CNT arrays [112], and GaAs [113] and ZnO nano-wire arrays [116] were fabricated using this process.

The fabrication of CNT arrays is a typical example of this mixed fabrication process (Fig. 51). Ordered arrays of CNTs were catalytically grown from the UTAM-patterned Ni nano-particle arrays on Si substrates. The CNTs are grown from the Ni particles with a one-to-one correspondence, i.e. each CNT is grown from a single catalyst particle. The high uniformity of the size of the Ni nano-particles (Fig. 51a1) results in an almost monodisperse diameter of the CNTs (Fig. 51b1). Moreover, the CNTs are found to be well-graphitized, which confirms the improvement of the crystalline quality. Fig. 52 shows GaAs [113] and ZnO [116] nano-wire arrays fabricated from Au nano-particle arrays. Similar to the CNTs, these nano-wires have a narrow distribution of the diameters. These large-scale free standing nano-wire and nano-tube arrays on substrates are desirable structures for future optoelectronic devices such as lasing and flat panel displays.

5.3. UTAM-assisted fabrication of ordered nano-ring arrays and the properties

Investigations on nanometer-sized rings of metals and semiconductors have attracted much attention recently due to their interesting features and properties such as the magnetooptical behavior in semiconductor nano-rings [146], and the persistent currents
tunable optical resonance [148], and circulating magnetic vortex structures [149] in metal nano-rings. In particular, ordered arrays of nano-rings are excellent candidate structures for high density magnetic recording systems.

5.3.1. Nano-rings prepared using sputtering and the magnetic properties

Hobbs et al. proposed an UTAM-assisted approach in fabricating ordered arrays of nano-rings on substrates [118]. There are two fabrication processes that are based on their approach (Fig. 53). In process I (Fig. 53a–c), an UTAM was placed on a thick layer of the desired ring materials that is covered with a 20 nm SiO$_2$ layer. An Ar$^+$ sputtering process deposited the ring material on the pore walls, forming nano-rings on the SiO$_2$ layer. The nano-rings that were fabricated using process I are usually short with low aspect ratios, such as the Ni nano-rings shown in Fig. 53g. Using process II, long nano-rings with high aspect ratios can be fabricated (Fig. 53d–f). The ring material was first evaporated into the UTAMs, forming nano-particles on the substrates and a top layer on the UTAM. The following Ar$^+$ sputtering process redeposited the evaporated material (nano-particles and top layer) on the pore walls. Finally, after the removal of the UTAM, free-standing nano-ring arrays were obtained. Fig. 53h shows Au nano-rings on a Si substrate that were fabricated using process II. Clearly the nano-rings have a relatively high aspect ratio.

Recently, Wang et al. investigated the spin dynamics of high-aspect-ratio Ni nano-rings in a longitudinal magnetic field [119]. The high-aspect-ratio Ni nano-rings were fabricated using the above-mentioned process II [118]. The magnetic field dependence of the spin waves measured by Brillouin scattering is in good agreement with the results by three-dimensional micromagnetic and macroscopic calculations. The simulated magnetization distribution within the high-aspect-ratio Ni nano-ring shows that under high magnetic fields, the rings show a single-domain state (termed as the “bamboo” state) where the spins are aligned parallel to the ring axis. When the magnetic field is lower than a critical field of 50 mT, the rings switch to a novel “twisted bamboo” state (Fig. 54a–d). In this state, the circulation directions of the spin components in the top and bottom planes of the rings are opposite, while in the middle planes the spins are parallel to the ring axis. The transition from the bamboo state to the twisted bamboo state corresponds to a local minimum in the dependence of the spin wave frequency on the magnetic field at about 50 mT (Fig. 54e).
5.3.2. Nano-rings and nano-spheres prepared using laser-assisted reconstruction

Kim et al. reported the fabrication of Au nano-rings and nano-spheres using a laser-assisted redeposition process [82]. First, using the UTAM nano-patterning process, Au nano-particle arrays were fabricated by pulsed laser ablation on substrates. In the meantime, an Au top layer formed on the UTAM. A subsequent cleaning process of the Au top layer using a low power laser illumination results in new nanostructures around the alumina pores. It is found that after 5 min illumination by a 55 mJ/cm² laser on the Au top layer, some Au evaporated into vacuum or into the pores of the UTAMs, leaving Au nano-spheres at the pore ends (Fig. 55a and b). In the case of using a 80 mJ/cm² laser for 5 min etching, more Au disappeared and finally Au nano-rings formed at the pore perimeters (Fig. 55c). Moreover, using the 55 mJ/cm² laser for a longer ablation time such as 10 min, similar Au nano-rings can be obtained. This indicates that the nano-sphere is an intermediate structure that occurs in the formation of the nano-ring. The formation of the
nano-spheres and nano-rings are thought to originate from the melting of the Au top layer and a subsequent reconstruction process on the top of the UTAM.

5.3.3. InGaAs nano-rings fabricated by selective area epitaxial growth

An integrated process in fabricating ordered InGaAs nano-ring arrays is reported by Chen et al. [117]. The process combines the UTAM nano-patterning approach and the selective epitaxial growth of InGaAs. A SiO₂ nano-porous mask was prepared on a GaN substrate using the UTAM nano-patterning. The epitaxial growth of InGaAs was
carried out on the SiO$_2$/GaN structure, and finally InGaAs nano-rings were obtained on the GaN substrate (Fig. 56a). The formation of the nano-rings depends on the successful transfer of the nano-holes to the SiO$_2$ mask and on proper growth conditions for the selective epitaxial growth. These ordered arrays of the uncapped InGaAs nano-rings show a strong PL at room temperature (Fig. 56b), which indicates strong confinement of the excitons in the nano-rings.

5.4. Nano-wire, nano-tube, and nano-pore arrays fabricated using UTAM-related processes

For device applications of one-dimensional nanostructure arrays, usually it is highly desirable to fabricate free-standing nano-wire or nano-tube arrays on substrates. Compared to the conventional alumina membranes (with a barrier layer and an aluminum layer), the connected UTAM on substrates with through pores is an excellent template to fabricate free-standing nano-wire or nano-tube arrays on substrates. So far different kinds of free-standing nano-wires and nano-tubes were obtained.

Some non-line-of-sight vapor-phase deposition processes, such as atomic layer deposition (ALD) [121], radio frequency sputtering [120], and microwave plasma-enhanced CVD [109], can produce nano-tubes in the pores of the UTAMs. ALD is a deposition process to fabricate highly conformal films on substrates. Using that process, Sander et al. prepared TiO$_2$ nano-tubes in the pores of connected UTAMs [121]. The PLD growth of the TiO$_2$ nano-tubes involved the repeated exposure of the UTAMs to TiCl$_4$ and H$_2$O vapors. TiCl$_4$ vapor reacted with the hydroxyl species on the pore walls, and the resulting TiCl$_x$ groups reacted with H$_2$O vapor to from Ti(OH)$_x$ groups, finally the Ti(OH)$_x$ groups condensed and formed TiO$_2$ on the pore walls. Fig. 57a and b shows free-standing TiO$_2$ nano-tube arrays on Si substrates. It is found that the tubes are open at the top but closed at the bottom (Fig. 57c and d).

Most of the nano-wires grown in the connected UTAM were prepared using wet-chemical processes such as the electrochemical and electroless deposition. Free standing nano-wire arrays have been fabricated on substrates, which include metals (Au [114,125,128], Ag [122], Cu [110], Ni [115] and Bi [124]), alloys (CoPt [123]), and semiconductors (BiTe [124] and Cu$_2$O [108]). The length of the nano-wires can be adjusted by changing the deposition
time, thus forming nano-wires with different aspect ratios. These ordered nano-wire arrays in UTAMs can also be used as building blocks for novel composite nanostructures. For example, Park et al. reported the fabrication of metal islands on Au nano-wires via the self-assembly of molecules [128].

Usually there are one or two metal interlayers between the substrate and the connected UTAM. These interlayers act as both adhesion promoter and electrode. It is found that the interlayer can also greatly affect the structures and properties of the deposited nano-wires. Yasui et al. prepared $L1_0$-ordered CoPt nano-wires in two kinds of connected UTAMs with different metal interlayer (W and Pt) [123]. The magnetic properties of the nano-wires fabricated on a W interlayer are quite different from the properties of the nano-wires on a Pt interlayer. The CoPt nano-wires on the W interlayer show random $c$-axis orientations while the nano-wires on Pt have a strong perpendicular magnetic anisotropy.

Using UTAM-related processes, it is possible to fabricate some other interesting nano-structures on substrates, such as ordered nano-pore arrays. Ding et al. recently prepared ordered ZnO nano-pore arrays through radio-frequency magnetron sputtering deposition on UTAMs [129]. Actually this ZnO nano-pore array is a top layer on UTAMs in the sputtering process (Fig. 58a and b). However, different to many other top layers on UTAMs, this ZnO nano-pore array is a highly crystalline-oriented top layer. The growth of this highly ordered ZnO layer on top of UTAMs originates from the localized negative charges on the top of UTAMs, which attract $Zn^{2+}$ ions and results in ZnO nucleation and growth on the top of UTAMs. It is found that the regularity of the ZnO top layer is largely
depended on the size of the UTAM pore walls. Thirty nanometres is around the best pore-wall size in obtaining highly ordered ZnO top layers. Moreover, by controlling the sputtering deposition process, multilayered ZnO nano-pores with similar morphology and height can be prepared. Fig. 58c, d, and e shows two, three, and four ZnO multilayers on UTAMs, respectively.

6. Summary and outlook

This review introduces the current state of the art concerning nano-patterning approaches that utilize ultra-thin alumina membranes (UTAMs). It is clearly shown that the UTAM nano-patterning is a promising approach in fabricating ordered arrays of surface nanostructures with controllable size and morphology and adjustable properties. The broad range of materials and structures that were fabricated using the UTAM nano-patterning indicates the high capability of this approach in creating ordered surface nanostructures. In the last 5 years, the research field of the UTAM nano-patterning has expanded very fast and already shows many new ordered surface nanostructures, which include ordered arrays of nano-particles, nano-holes, nano-spheres, nano-rings,
nano-wires, and nano-tubes. These surface nanostructures present interesting properties that can be used in many application fields in optics, electronics, optoelectronics, magnetism, and sensing. Some of these properties are tunable based on the adjustment of the UTAM-related fabrication processes and the structure parameters of the nanostructures. Due to these interesting and tunable properties, some of the UTAM-fabricated surface nanostructures are close to being incorporated into nano-devices (e.g. the MIS memory devices fabricated using ordered Ge nano-particles [51]).

As a new research field, some basic and important topics in the UTAM nano-patterning have not been completely investigated yet. So far the property tuning of the ordered nanostructure arrays based on the adjustment of the size, spacing, and shape of the nanostructures has not been studied systematically. The adjustable structural parameters of the UTAM-fabricated nanostructures are among the most attractive advantages of the UTAM nano-patterning approach. By changing the size, spacing, and shape of the nanostructures, the properties of the nanostructure arrays can be adjusted, hence realizing an active property tuning of the nanostructures. Future research of the UTAM nano-patterning should focus on the property tuning based on the adjustment of the structural parameters of the nanostructures.

The usual way to study the property tuning of the nanostructures is to measure and analyze the macroscopic properties of the arrayed nanostructures with different structural parameters. This is a relatively convenient but indirect investigation of the relationship between the properties of the ordered nanostructure arrays and the parameters of the nanostructures. Moreover, it is difficult to obtain a precise tuning of the properties based on the adjustment of the structural parameters. An ideal way to investigate the property tuning of the arrayed nanostructures is to study the microscopic properties of the basic component of the nanostructure arrays – the individual nanostructure, and the interaction of the adjacent nanostructures. Because the UTAM-fabricated surface nanostructures have high regularity, the arrayed nanostructures have similar size, shape, crystalline structure, and ambient condition. Thus it is possible to analyze the macroscopic properties of the nanostructure arrays based on the integration of the microscopic properties of the individual nanostructure and the interactions of the nanostructures. Using this property investigation method, knowledge on the direct relations between the properties and the structural parameters of the nanostructures can be gained, and thus the properties of the ordered nanostructure arrays can be controlled. Once the precise tuning of the properties of the nanostructure arrays based on the adjustment of the parameters of the individual nanostructure can be obtained, the door to the fabrication of nano-devices with adjustable properties and performance can be completely opened.

Another challenging issue for future research in the field of the UTAM nano-patterning is the fabrication of UTAM-related advanced composite architectures with novel and improved properties. Most surface nanostructures prepared using the UTAM nano-patterning, such as the nano-particle or nano-hole arrays on substrates, can be good functional parts of advanced composite architectures. Some examples of advanced composite architectures with improved properties include high-quality device-level GaN layers grown on ordered GaN and SiO2 nano-hole arrays [102,103], metal/oxide core–shell nano-particles oxidized from ordered metal nano-particle arrays [49], and electrolyte–molecule–silicon nano-capacitors in Si nano-hole arrays [104]. Future efforts in fabricating UTAM-related composite architectures are expected to result in more advanced nanostructures with novel and interesting properties that are suitable for nano-device applications.
The UTAM nano-patterning approach is an efficient and low-cost method in fabricating large-area nanostructure arrays with high density. This makes the UTAM nano-patterning approach very suitable for fabricating ordered nanostructures for high-density magnetic recording devices and high-sensitivity sensors. However, so far the study on the UTAM-fabricated magnetic metal and alloy nano-particle arrays is limited. In the future, the research interests in the magnetic properties of the ordered nanostructure arrays will increase fast in the UTAM nano-patterning field.

It should be mentioned that the lack of long-range ordered pores of the self-organized alumina masks limits the applications of the UTAM-fabricated surface nanostructures, especially in some areas such as storage devices that require a long-range order of the surface nanostructures. Although UTAMs with long-range ordered pores can be fabricated using the pretexturing (imprinting) process, it is quite expensive and time-consuming to obtain the imprinting molds. Therefore, it would be highly desirable if an improved pretexturing process (with cheap molds) or a novel method could be designed to fabricate long-range ordered UTAMs.

In essence, we anticipate that the young research field of the UTAM nano-patterning will continue to expand fast and will enable the development of more advanced surface nanostructures with unique and attractive properties.

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References


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