FPGA-accelerated Adaptive Optics Wavefront Control

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ABSTRACT

The speed of real-time adaptive optical systems is primarily restricted by the data processing hardware and computational aspects. Furthermore, the application of mirror layouts with increasing numbers of actuators reduces the bandwidth (speed) of the system and, thus, the number of applicable control algorithms. This burden turns out a key-impediment for deformable mirrors with continuous mirror surface and highly coupled actuator influence functions. In this regard, specialized hardware is necessary for high performance real-time control applications.

Our approach to overcome this challenge is an adaptive optics system based on a Shack-Hartmann wavefront sensor (SHWFS) with a CameraLink interface. The data processing is based on a high performance Intel Core i7 Quadcore hard real-time Linux system. Employing a Xilinx Kintex-7 FPGA, an own developed PCIe card is outlined in order to accelerate the analysis of a Shack-Hartmann Wavefront Sensor. A recently developed real-time capable spot detection algorithm evaluates the wavefront.

The main features of the presented system are the reduction of latency and the acceleration of computation. For example, matrix multiplications which in general are of complexity $O(n^3)$ are accelerated by using the DSP48 slices of the field-programmable gate array (FPGA) as well as a novel hardware implementation of the SHWFS algorithm. Further benefits are the Streaming SIMD Extensions (SSE) which intensively use the parallelization capability of the processor for further reducing the latency and increasing the bandwidth of the closed-loop. Due to this approach, up to 64 actuators of a deformable mirror can be handled and controlled without noticeable restriction from computational burdens.

Keywords: adaptive optics, PCIe, FPGA, deformable mirror, laser material processing, Linux real-time system, wavefront sensor

1. INTRODUCTION

Fast changing turbulence imposes wavefront aberrations in free-space propagation. These wavefront aberrations need to be measured 5 to 20 times faster than they occur, calling for measurement rates around 1 kHz and a feedback loop operating with at least several hundred Hz (better kHz).\textsuperscript{1,2,3} Control setups have been implemented based on (real-time) PC\textsuperscript{2,3,4} in adaptive optical test benches that apply at least one deformable mirror and a Shack-Hartmann wavefront sensor. The papers report wavefront sampling frequencies of up to 800 Hz with control-loop frequencies between 50 and 260 Hz. Highest sampling frequencies of 20 kHz have been shown\textsuperscript{5} where only the wavefront is measured without closing the control loop. The increase of the sampling rate to 20 kHz as well as a resolution of $512 \times 512$ pixel, 14-bit monochrome, implies that each second, roughly, 8.6 GByte pixel information has to be evaluated. To transfer this amount of data in real-time from the camera to a computer would require PCIe 2.0 x32 which has a transfer rate of 16 GByte/s. But without any pre-processing of the data it is not feasible to process this amount of information in real-time, unless an FPGA or an ASIC (application-specific integrated circuit) evaluates the image data. For the evaluation of the controller in the closed loop, rapid prototyping control (RCP) approaches are highly recommended. Here, the wavefront is selectively deformed by a

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deformable mirror. A second deformable mirror and a tip/tilt mirror serve for the compensation of the wavefront deformation by applying new control algorithms on the presented hardware concept. A schematic overview of the developed rapid prototyping adaptive optical setup is given in Fig. 1. The speed and accuracy conditions demand for high-performance real-time control of the wavefront.

The speed of real-time adaptive optical systems is primarily restricted by the acquisition rate of the wavefront sensor, data processing hardware, and computational aspects. Due to a huge number of actuators the arising complexity problem for controlling the mirror entirely is very demanding when no decoupling, at least locally, is possible. A lot of approaches live on the assumption that the actuators may be decoupled, see e.g. the PID approach in 6.

This assumption, in general, is valid especially for segmented deformable mirrors and only restricted to continuous deformable mirrors, particularly, when there is no co-located displacement sensor. Whenever decoupling is not possible or inappropriate, the application of distributed/decentralized control is limited. Furthermore, any noticeable delay dramatically degrades the performance of the control-loop and may complicate the proof of stability, significantly. Thus, a low latency hard real-time system with high computation power is substantial for obtaining high performance.

The goal of our work is to setup and evaluate a real-time capable, rapid control prototyping system in order to be able to test new control approaches within acceptable time. The RCP system is based on a Shack-Hartmann wavefront sensor (SHWFS) with a CameraLink interface whose signals are fed into an FPGA card to compute and output the deformable mirror control signals, see Fig. 1 and 2. Additionally, a special adaptive optical test bench is developed for the experimental evaluation of velocity and accuracy within the control loop. Therefore, pre-defined aberrations (e.g. Kolgomorov turbulence) are imposed on the wavefront by a deformable mirror. A second deformable mirror and a tip/tilt mirror both serve to compensate for these aberrations.

![Figure 1. Demonstrator - Deformable Mirror with compact control loop](image)

It is one characteristic of high-speed real-time adaptive control that for being able to compensate for disturbances the wavefront has to be measured with an adequate measurement rate. In our experiments, an SHWFS is used for a high-speed wavefront acquisition with 905 Hz. Regarding the control system, the bandwidth of a closed-loop system is limited, in general, by the maximum measurement-rate, the maximum possible controller frequency, and the individual characteristic dynamics of each component of the plant. In our case, the plant is the series connection of deformable mirror, optical transfer path, wavefront sensor, and wavefront analysis/reconstruction.

Since the disturbance is obtained by evaluation of the wavefront camera signal, the readout and data processing of the wavefront sensor crucially determine the possible performance of the overall system.
In view of the required high-data bandwidth and the importance of low-latency with high-throughput, the deployment of an FPGA is appropriate. FPGA systems are beneficial for their capability to process a huge amount of tasks in parallel that are limited only by their quantity of slices (area of the FPGA) or the intrinsic problem of parallelizing a task. The maximum clocking frequency of an FPGA is in almost all cases distinctly lower than the clocking rate of a modern processor such as a Core i7 from Intel. Nevertheless, for image processing in most cases this is not relevant because the transmission of the image from the camera is below the critical clocking frequency of an FPGA and the time critical parts may be parallelized so as to achieve higher throughput with lower latency/delay. For that reason, the past years have generated many publications on the use of FPGA’s for the evaluation of an SHWFS or even on the use of FPGA’s for controlling the adaptive optics system entirely.7–9

Our concept differs already decisively in the fundamental approach: We present/develop a system that may be operated as an RCP system as well as a stand-alone system. The delay/latency from the SHWFS is reduced extensively while even increasing the framerate.10,11 Therefore, the main contributions of the paper are the introduction of a rapid prototyping system that shows reduced delay/latency and accelerated computation, and further allows for its evaluation with the recently developed adaptive optical test-bench.

The paper is organized as follows: Section 2 presents the proposed rapid control prototyping FPGA concept with its different components. In Section 3 the experimental setup is exposed in detail. Section 4 is devoted to the conclusions and gives on outlook to some forthcoming works.

2. HARDWARE CONCEPT

For minimizing the design effort, a rapid control prototyping (RCP) approach is implemented so as to quickly test the control algorithms and iterate towards a further improvement of performance. For this purpose, we have decided to develop a custom FPGA board to serve as the basis of the platform for incorporating the specific aspects of adaptive optics.

The following section is devoted to present the FPGA board, used adapter boards, and the developed real-time interface concept in detail. The proposed concept is to replace the currently employed solution which was presented and used.12,13 As far as it is appropriate in the design, all disposable features of the PXI LabVIEW solution shall be maintained or further improved, e.g. the pinout of the VHDCI connectors are compatible. For obtaining the flexibility of an RCP system the concept is either usable as stand-alone system or may be integrated into a performance computer for more flexibility. For being independent of expensive and intricate hardware, except for the own developed boards, the RCP resorts to real-time Linux as the operating system. The aim is to have a system which shows a better performance when compared with the presented PXI system, has a lower cost, and will allow the entire control over any process. It is clear that the solution needs to be specialized for high-performance control of adaptive optics and shall not strive to replace existing high-performance (in general commercial) rapid prototyping solutions as for example dSPACE.

The basis of the proposed concept is a Xilinx Kintex-7 FPGA. This FPGA handles the communication to the host computer (if needed) via PCIe and interfaces to the SHWFS (Imagine Optics Haso3 Fast) via CameraLink. The developed boards are designed in the PCIe form factor such that they may be directly plugged into a computer housing. An overview over the whole concept with all components is given in the block diagram of Fig. 2 where all analog signals are drawn in bold.

DM1 is a deformable mirror with thirteen piezoelectric actuators that is used to generate specific disturbances which are then compensated by a tilt/tilt and a second deformable mirror (DM2). We employ tilt-mirror S-330.2SL from Physik Instrumente (PI). Each degree of freedom is controllable via a ±10 V signal. DM2 has 41 piezoelectric actuators, and incorporates thermal sensors as well as integrated heaters.14,15 DM2 is a specially designed deformable mirror to be implemented in high-power laser systems. The laser-induced mirror deformation is compensated by controlled mirror heating as shown.16 The mirror offers mirror membrane buried functionality, e.g. five thick-film heaters and nine thick-film temperature sensors.

*PCI Express (Peripheral Component Interconnect Express), officially abbreviated as PCIe, is a high-speed serial computer expansion bus standard designed to replace the older PCI.
The HV64 is an amplifier with 64 channels for piezoelectric actuators. Additionally, the HV64 incorporates a front-end for amplifying low current/voltage signals of the thermal sensors. The thermal sensors are amplified by the HV64 and then captured by the ADC board. To support up to 32 analog channels, a digital signal is available which controls the integrated analog multiplexer of the HV64. Therefore, with only 16 analog channels, 32 analog signals may be captured. The integrated heaters are controlled via external power supplies where each power supply consists of three buck-converter to compensate for the different temperatures of the deformable mirror. The performance computer receives the slope information which are calculated out of the Haso3 Fast image with an FPGA. With this information the control signals are computed. Therefore, an FPGA board, two DAC boards, and one ADC board are designed and setup.

### 2.1 DEVELOPED BOARDS

#### 2.1.1 FPGA BOARD

The heart of the concept is an FPGA board which is connected to two DAC (digital to analog converter) boards and one ADC (analog to digital converter) board. The FPGA board may communicate over PCIe 2.0 x4 with the real-time Linux system. PCIe 2.0 x4 is able to transmit and receive 2 GByte/s (fully duplex-capable). Furthermore, the FPGA board provides a CameraLink interface to be able to analyze an external SHWFS directly in hardware for increasing the throughput as well as for reducing the latency. For configuring the SHWFS and for programming the FPGA, a FTDI FT2232H chip is used.

An extra Ethernet interface capable of 10/100/1000 Mbit is available so as to stream the data to an other computer, e.g. for monitoring the wavefront or to connect further components. The spots of the SHWFS may be displayed via standard VGA interface without any intervention by the computer. For status information, eight LEDs are allotted.

A mini Displayport with transition-minimized differential signaling (TMDS) is present for high-resolution video output or to extend the existing solution with other components which require a high-speed interconnection, e.g. an own developed SHWFS based on the Imagine Optics CP80-3-M-540 camera which does not have a CameraLink interface.

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1. TMDS is a technology for transmitting high-speed serial data and is used e.g. by the HDMI video interface as well as on other digital communication interfaces.
The FPGA plugged on the board is a TE0770/TE0741/TE0720 micromodule from Trenz electronics. The TE0770 and TE0741 both are based on a Xilinx Kintex-7 in different packages with slightly different external components such as DDR3-SDRAM. The micromodule TE0720 employs a Xilinx Zynq-7000 that incorporates a dual-core Cortex-A9 processor equipped with double-precision floating-point-extensions connected to an Xilinx Artix-7 FPGA. The TE0720 allows the use of the developed FPGA board as stand-alone with embedded Linux operating system. The micromodules have been used because they are appropriate to reduce the effort during designing and producing the FPGA boards. The application of the modules reduces the overall cost and allow to minimize the development time. Furthermore, the exchangeability of the modules is useful if different speed-grades and/or sizes of the FPGA’s are needed or in case of any malfunction incidence.

**Figure 3. Block diagram of the PCIe FPGA concept**

### 2.1.2 ADC BOARD

The ADC board is a separate board which handles the capturing of the analog signals of the nine temperature sensors via two parallel eight channel ADS1178 16 bit analog digital converters from Texas Instrument. If a higher resolution is desired, the ADS1278 with resolution of 24 bits may be used instead. The block diagram of the ADC board is shown in Fig. 4.

The analog to digital converters have a resolution of 16 bit and a separate digital signal is available to drive an external multiplexer such that in total 32 analog channels may be captured. Each analog input is decoupled with an operational amplifier for impedance adjustment of the input and to guarantee the conditions of Shannon’s theorem (sampling must be done at least two times the maximum occurring frequency). The maximum sampling frequency of the analog digital converter is configurable with the FPGA up to 125 kHz in pre-specified steps. The connections of the analog digital converter to the FPGA are realized via Serial Peripheral Interface (SPI). Each channel can be enabled and disabled, separately. A down-sampling as well as a further filtering of the acquired signals are also provided in the FPGA. The analog inputs are used for monitoring the integrated temperature sensors.

Additionally, two external power supplies drive the buried heater to manipulate the thermal gradient and to compensate for laser-induced deflections of the deformable mirror. Each power supply has three individual channels and may be interfaced via RS232. The individual protocol implementation of the power supply is realized with a micro-controller. For simplicity, the FPGA sends data to ATxMEGA which then addresses the two external power supplies over two individual RS232 interfaces. Error handling and surveillance of the external power supplies are implemented in the micro-controller to be more flexible and to have lower implementation effort in the FPGA.

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‡DDR-SDRAM means double data rate synchronous dynamic random-access memory which is a class of memory integrated circuits used in computers.
2.1.3 DAC BOARD

Two separate DAC boards are used for controlling the piezoelectric actuators of the deformable mirrors (DM1 and DM2) and the tip-tilt mirror. In total 64 analog channels are provided. 62 of them are driven by an intercalated amplifier (HV64) and two are amplified by the TT-amplifier (PI E-505.00) with the corresponding controller module (PI E-509.X3). Each card has 32 individual analog channels with a maximum output voltage of ±10 V with 16 bit resolution. Fig. 5 shows the block diagram of the DAC board. One DAC board consists of four digital to analog converters AD5362 from Analog Devices which have a programmable gain and output span. Therefore, the resolution is not affected when only 0 – 10 V output is needed as for the HV64. The power supply of ±12 V is generated with a DC/DC converter TES-1222 from Tracopower and an ultraprecision low noise voltage reference with +5 V is used as a reference.

2.1.4 CONSTRUCTED BOARDS

Fig. 6 depicts all boards connected to the JTAG Debugger for programming the FPGA via Xilinx ISE Design Suite. All boards were successfully tested for functionality, also with specific VHDL implementation for the DAC.

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3Joint Test Action Group (JTAG) is the common name for the IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture and was initially developed for testing and programming printed circuit boards.
and ADC card. The implementation of the SHWFS evaluation was ported from the Xilinx Spartan-6 FPGA to the Kintex-7 with success and a further increase of the performance. The maximum clocking frequency of the SHWFS evluation has been increased to above 150 MHz.

Figure 6. experimental setup - all boards together and connected

### 2.2 Real-Time Linux

As has been motivated before, a real-time Linux operation system is deployed. Nowadays, various Linux kernel patches are available to guarantee real-time behavior, e.g. RTLinux, Xenomai, and RTAI, to name but a few. These approaches differ considerably in their implementation and each of them has advantages and disadvantages. For our approach, RTAI turns out to be the most suitable due to the fact that the control algorithm may be synthesized out of the MATLAB/Simulink model via Simulink Coder, formerly Real-Time Workshop. This feature is very useful during testing and developing control algorithms because it is not necessary to program the controller manually in C/C++ or any other programming language. The code then operates via RTAI-Lab, and the monitoring of the different signals and model parametrizations can be done graphically. The performance decrease is very limited and may be avoided almost entirely when the code is ported to kernel space.

In view of these benefits, the proposed setup is well-taylored as an RCP system while remaining rather inexpensive.

#### 2.2.1 Real-Time Application Interface

RTAI is the acronym of Real-Time Application Interface and is an extension of the Linux Kernel which grants the possibility to write applications with strict timing constraints. Due to the extension, deterministic response to interrupts is guaranteed when LXRT is used. LXRT allows to use all the services made available by RTAI in user space, both for soft and hard real-time.

This allows the use of Linux’ protecting mechanism without noticeable impact on latency and overhead. If the application runs in kernel space, then programming errors may let crash the entire system and the debugging is very time-consuming and complicated.

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"Most modern computer operating systems segregate virtual memory into kernel space and user space. Kernel space is strictly reserved for running a privileged kernel, kernel extensions, and in general most of the device drivers. The user space, in contrast, is the memory area where application software and some drivers are executed."
Nowadays, RTAI use the Adeos kernel patch to achieve real-time behavior. Also, it is free of patent issues (status 12/2013). Fig. 7 illustrates the RTAI principle. The bypassing of the interrupts is realized with the Real-Time Hardware Abstraction Layers (RTHAL). As long as the RTAI modules are not loaded, case A is active. Interrupts are handled the same way as in a standard Linux system. If the RTAI modules are loaded then case B is active and the interrupts are assigned to the real-time extension but the interrupts are also forwarded to the RTHAL.

2.3 Comedi

Interfacing the FPGA PCIe board requires a driver which runs in kernel space. In this regard, Comedi is an interesting open-source project which offers a comfortable platform for the management of different data acquisition cards and the development of own drivers for convenient hardware. The drivers are implemented as core Linux kernel module which provide a common functionality while comprising individual low-level driver modules.

Comedi shows the benefit to be applicable form user-space via Comedilib such that testing or generating patterns may be done manually without using kernel space applications. A lot of features have already been implemented within Comedi which thus may be adopted as it stands.

The driver for the PCIe interconnection of the FPGA board is realized within Comedi to be directly compatible to RTAI-Lab and to benefit from Comedi’s framework. Fig. 8 shows the device hierarchy of the implemented device driver for the PCIe FPGA board.

2.4 QTScope

For testing, adjusting, and simple experiments it is important to have the facility to directly monitor the results from the SHWFS and the analog inputs. In addition, constant analog outputs or sine waves need to be realizable without using Simulink Coder to generating the code for RTAI-Lab each time.
QTScope was created in 2003, originally to be able to display analog inputs. For our purpose it was forked and ported to QT4, see https://github.com/steffenmauch/QTScope. QTScope employs the comedi interface based on the userspace library comedilib. To be able to directly visualize the SHWFS results, a plugin for QTScope has been programmed, see Fig. 9 and 10. Fig. 9 displays the slopes of the SHWFS. A reference can be loaded to zero the slopes. Fig. 10 shows the case when out of the acquired slopes the wavefront is reconstructed by zonal reconstruction.

2.5 Simulink Coder/Matlab

For designing and testing different controllers for the adaptive optical system, Matlab and Simulink, resp., provide very helpful tools. There exists a real-time target for Simulink Coder in order to generate out of a Simulink model directly the code which is then able to run in real-time with RTAI. This process is visualized in Fig. 11. Simulink Coder compiles the simulink model into a rtw file, which is then further processed by the Target Language Compiler. The last step is done by ‘make’, which then generates the real-time executable.

Apart from that and as an alternative, Scicos may also be used for controller simulation and generation of open-source real-time code. With the work flow shown in Fig. 11 the simulation model may be directly run in real-time without time consuming and error prone porting.

Furthermore, e.g. matrix multiplication may be accelerated by using the Streaming SIMD Extensions (SSE) or Advanced Vector Extensions (AVX) of the multi-core processor (Intel Core i7). One may either rely on the capability of the compiler to use the processor extensions or the matrix multiplication is realized as an extern C/C++ s-function in Simulink which forces the processor to use the available extensions, if possible.

There are some disadvantages of the extension, e.g. a specific memory layout is required for the data and furthermore overhead comparing to standard instructions are possible because of context switches. Nevertheless, for huge matrix multiplications making use of the extension usually results in a large performance benefit.

1 Qt is a cross-platform application framework that is widely used for developing application software with a graphical user interface.

2 Scicos is a graphical dynamical system modeler and simulator, free of charge.
It is also possible to accelerate the matrix multiplications by swapping the computation to the FPGA via C/C++ s-functions. This s-function transfers the matrices to the FPGA via PCIe and the FPGA use its DSP48 slices to calculate the result in parallel. Afterwards, the result is transferred back to the real-time program, again via PCIe.

3. EXPERIMENTAL SETUP

3.1 ADAPTIVE OPTICAL TESTBENCH

The adaptive optics test-bed has been designed to set-up and evaluate the FPGA-based AO-control loop. To this end, we incorporate a deformable mirror serving as an aberration generator (DM1), and further a tip/tilt mirror, and a second deformable mirror (DM2) to compensate for the imposed aberrations. The experimental setup is shown in Fig. 12. A HeNe-Laser emitting at 633 nm is collimated and its beam is adapted by a lens telescope. The beam is limited by an aperture to match the 20 mm aperture of the first deformable mirror (DM1) that selectively aberrates the beam. A subsequent 1:1 telescope projects the aberration plane of the first mirror on the tip/tilt which redirects the aberrated beam to the compensation mirror (DM2). A second 1:1 telescope projects the tip/tilt surface on the compensation mirror such that the planes of the three deformable mirrors are...
conjugated. The beam is incident on the mirrors on a small angle of 8° so as to allow only low system induced aberrations.

We use two SHWFS for characterization: a slow, high resolution, large dynamic range SHWFS (SHSLAB - HR 130, Optocraft GmbH, WFS2) for verification of the proper adjustment of the AO test bed and a fast, low resolution, low dynamic range SHWFS (HASO3 fast, Imagine Optics, WFS1) for the control-loop. Therefore, the beam is focused after the last deformable mirror, divided by a beam splitter cube, and collimated by different lenses to match the SHWFS apertures. The measurement apertures are conjugated to the mirror apertures.

4. CONCLUSION

We have presented a novel FPGA-based adaptive optics concept that allows to fully exploit the performance of an adaptive optics framework while featuring a rapid control prototyping system. Methods for evaluating the spots of an SHWFS with an FPGA may now be developed specifically for increasing the setup’s performance to a large extent. For this new setup, a novel approach for evaluating the wavefront with an FPGA is presented in[10,11] where a reduction of evaluation time in the SHWFS by more than half of the original delay—formally 3 ms reduced to 1.5 ms—has been demonstrated. Demonstrated by simulation studies, the decrease of latency to 1.5 ms of the SHWFS may yield an overall increase of bandwidth to about 350 Hz instead of the formerly achieved 100 Hz.[13]

In addition, each analog output signal has the same phase, enforced by the implementation in the FPGA. In this way, time-varying delays are avoided and the usual bottleneck, i.e. the delay induced by the SHWFS, is reduced to a minimum. The above-proposed system setup comprises enough computational power such that no limitations are to be expected.

So far, each individual component has been tested. The ADC boards have been verified to be able to output in parallel, analog signals with frequencies above 10 kHz, reliably. First tests have been conducted with the integrated heaters of DM2 while using the ADC board to drive the external high-voltage power supplies. The PCIe interconnection of the FPGA board has been tested thoroughly and verified to work also reliably. The integration of the driver for the FPGA board into Comedi has reached a viable state.

Next steps of investigation are thus to compare former results with the results that may be achieved with the new concept so as to plumb the maximum performance of the experimental setup.

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